

FIG. 1

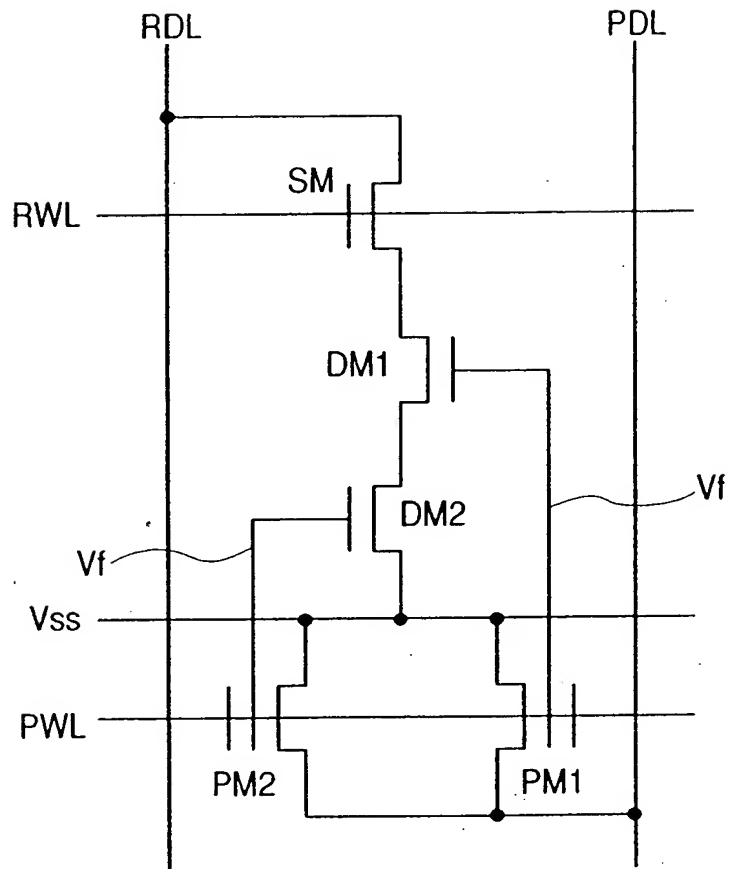


FIG. 2

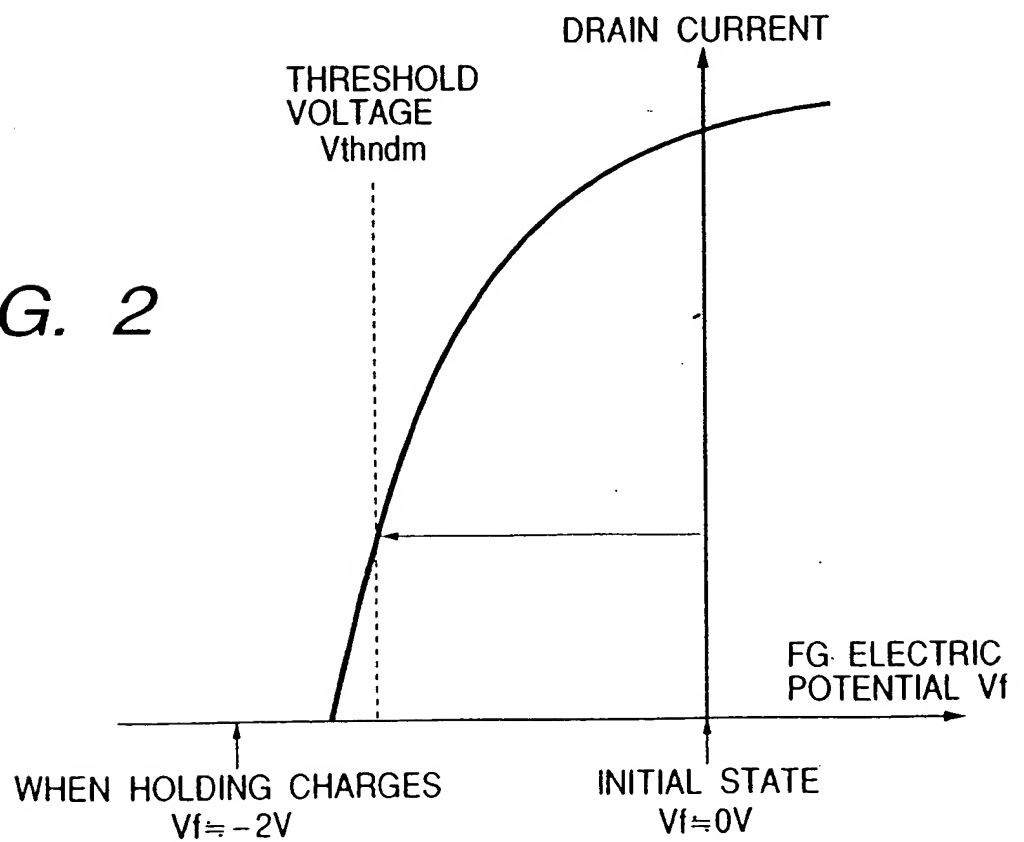
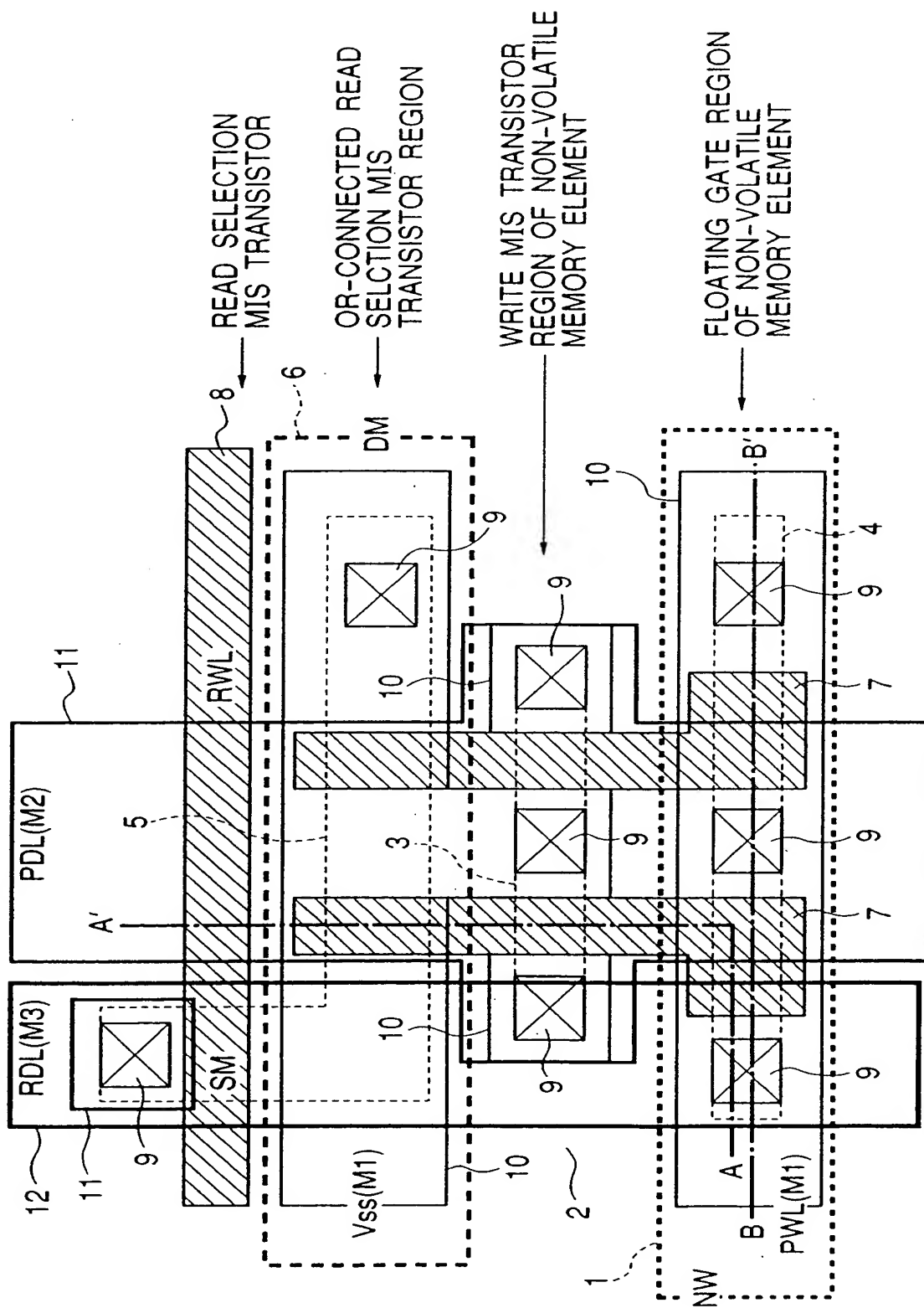


FIG. 3



**FIG. 4**

CROSS SECTION TAKEN ON LINE A-A' IN FIG. 3

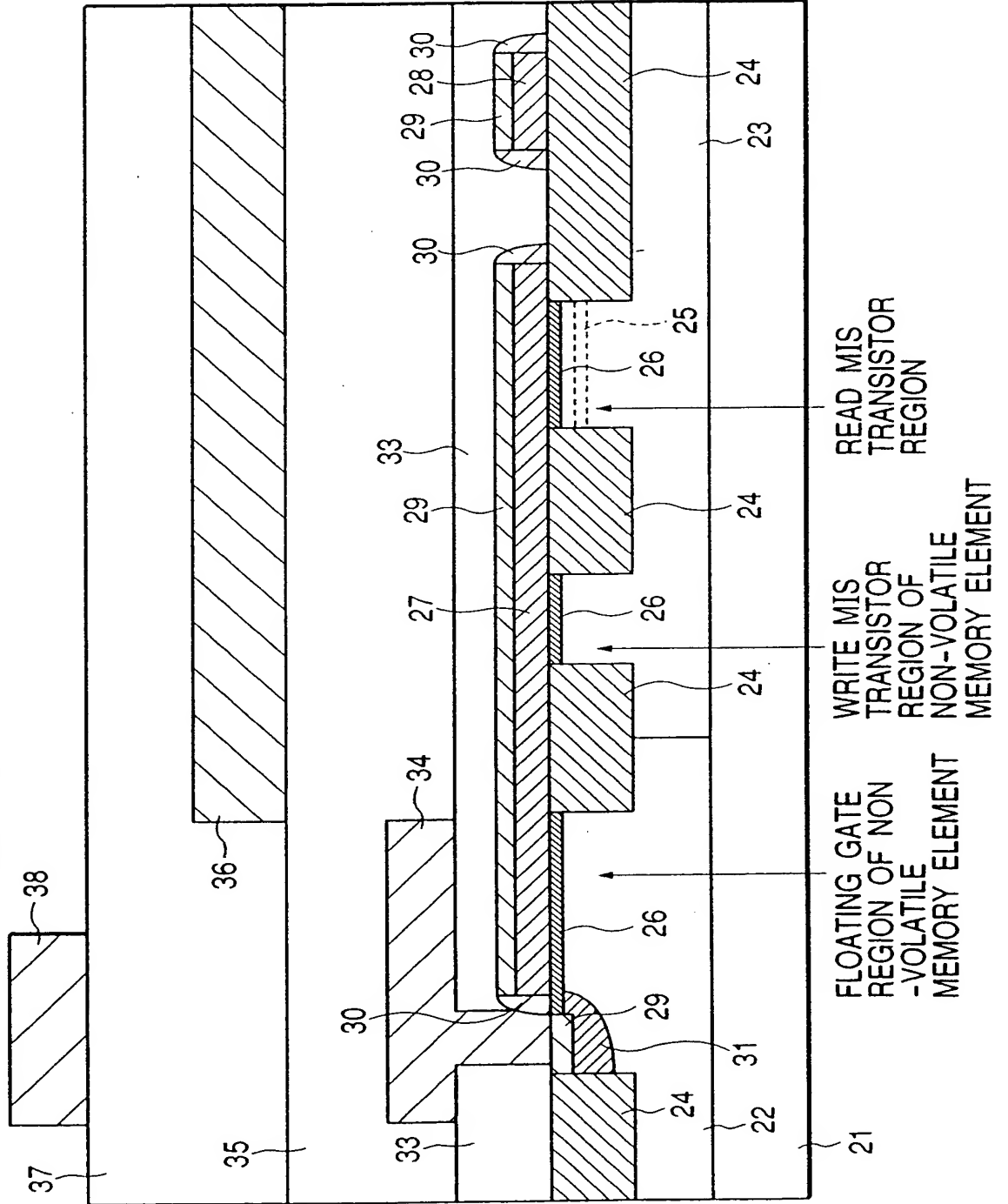


FIG. 5

CROSS SECTION TAKEN ON LINE B-B' IN FIG. 3

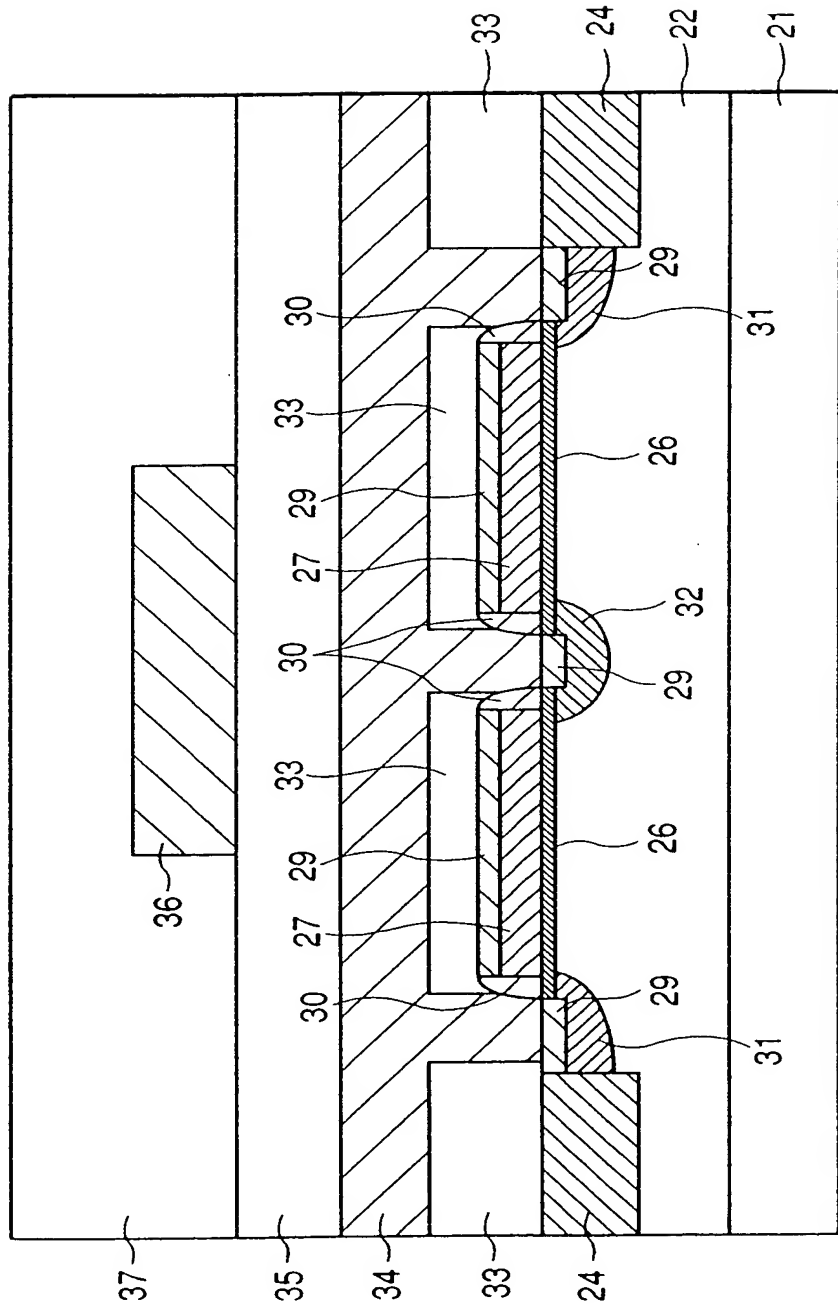
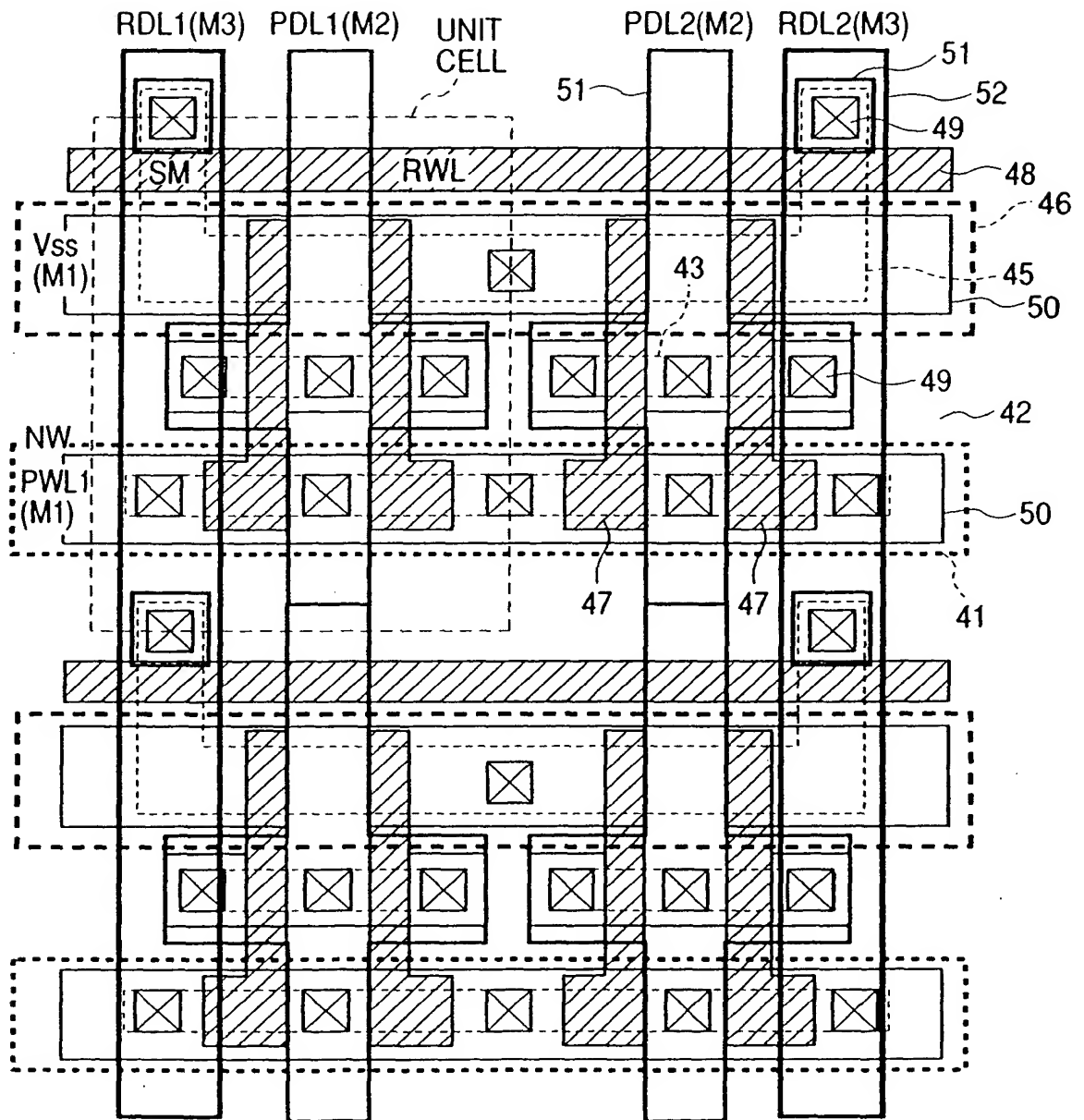


FIG. 6



*FIG. 7*

	PDL	PWL	RDL	RWL	Vss
WRITE	5V	5V	0V	0V	0V
ERASE	0V	0V	0V	0V	6V
READ	0V	0V	1.8V	1.8V	0V
HOLD	0V	0V	0V	0V	0V

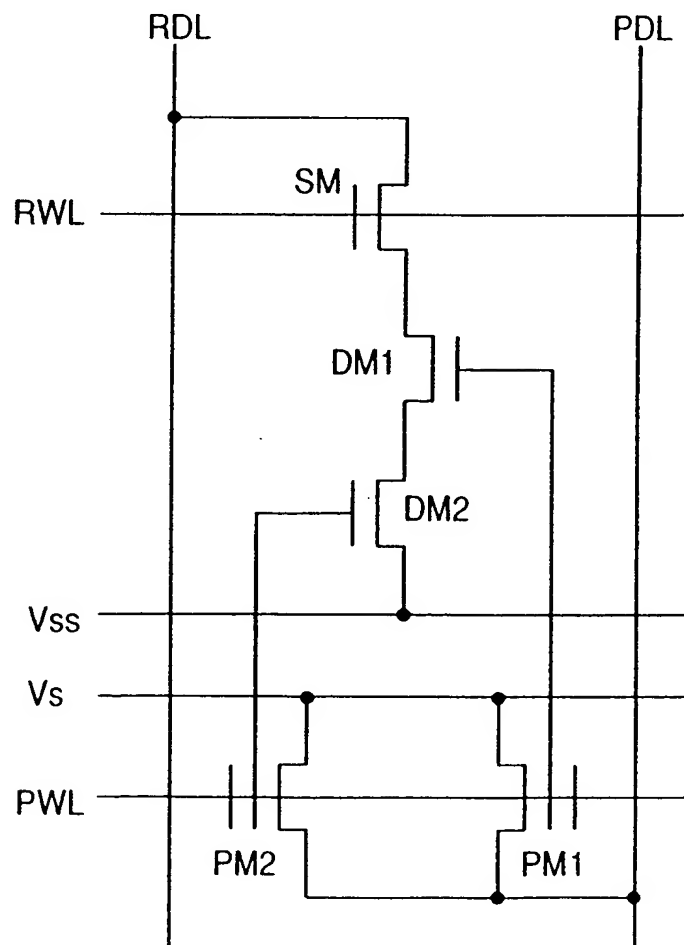
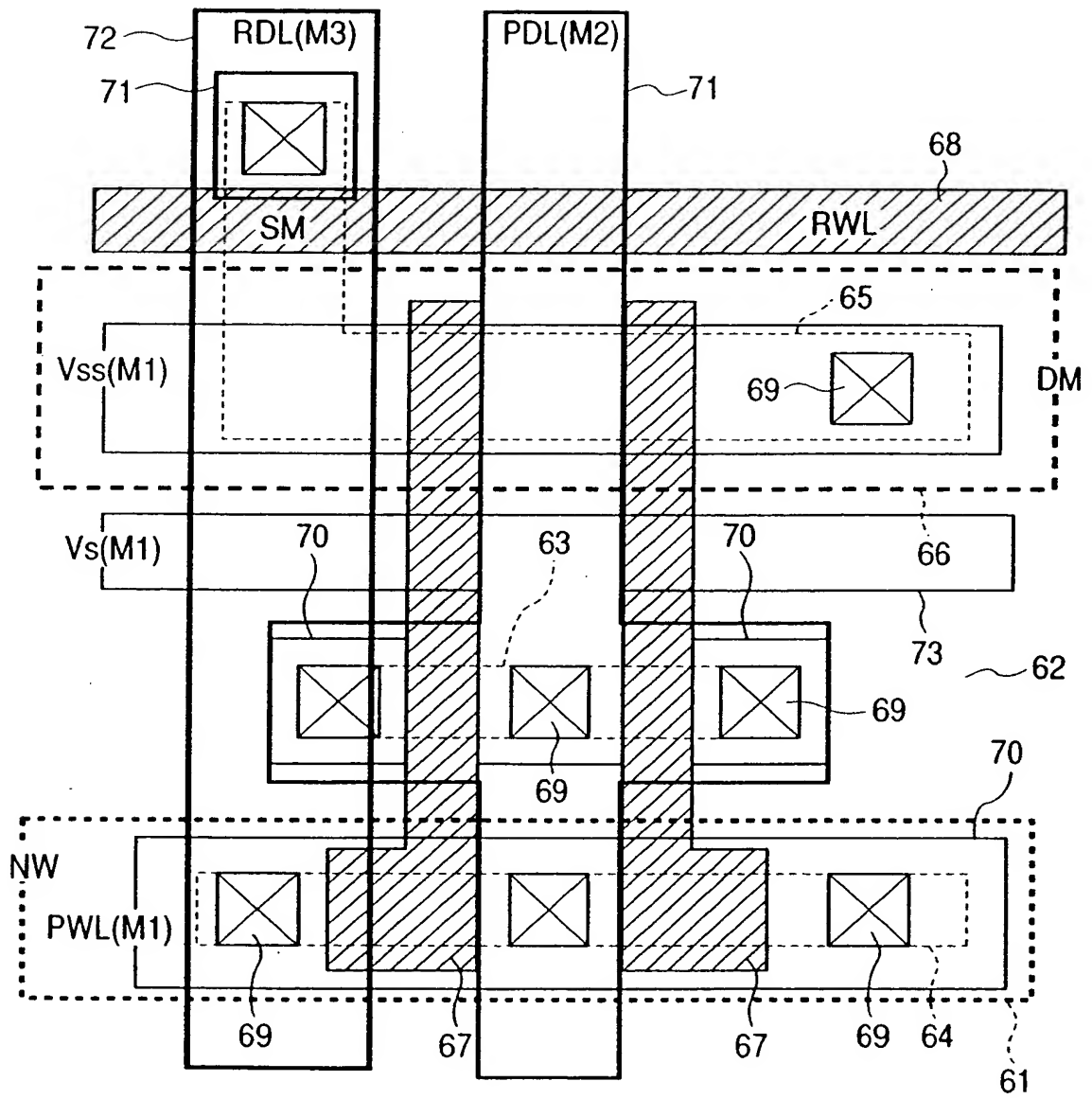
*FIG. 8*

FIG. 9



*FIG. 10*

	PDL	PWL	RDL	RWL	Vs	Vss
WRITE	5V	5V	0V	0V	0V	0V
ERASE	0V	0V	0V	0V	6V	0V
READ	0V	0V	1.8V	1.8V	0V	0V
HOLD	0V	0V	0V	0V	0V	0V



FIG. 11

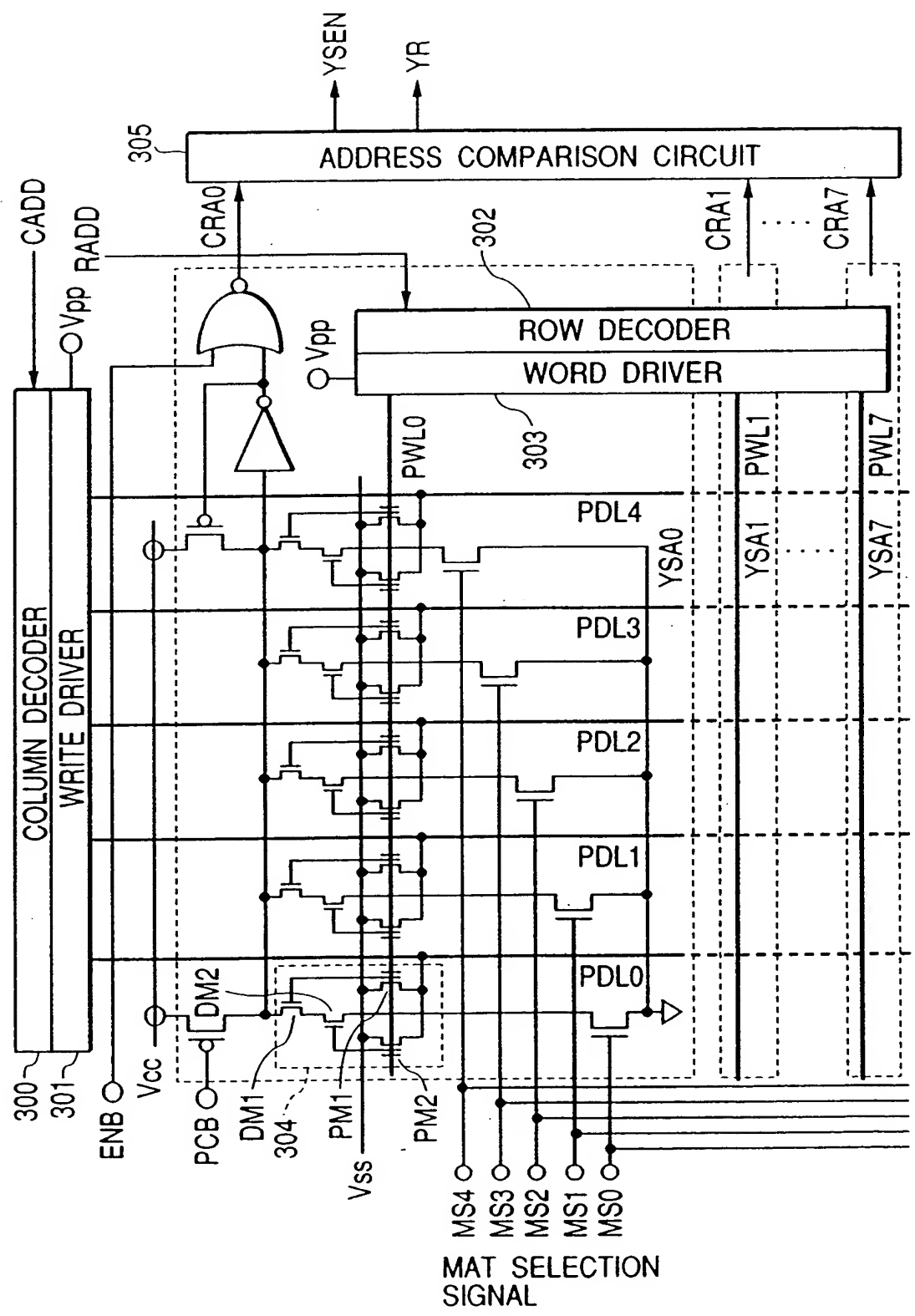


FIG. 12

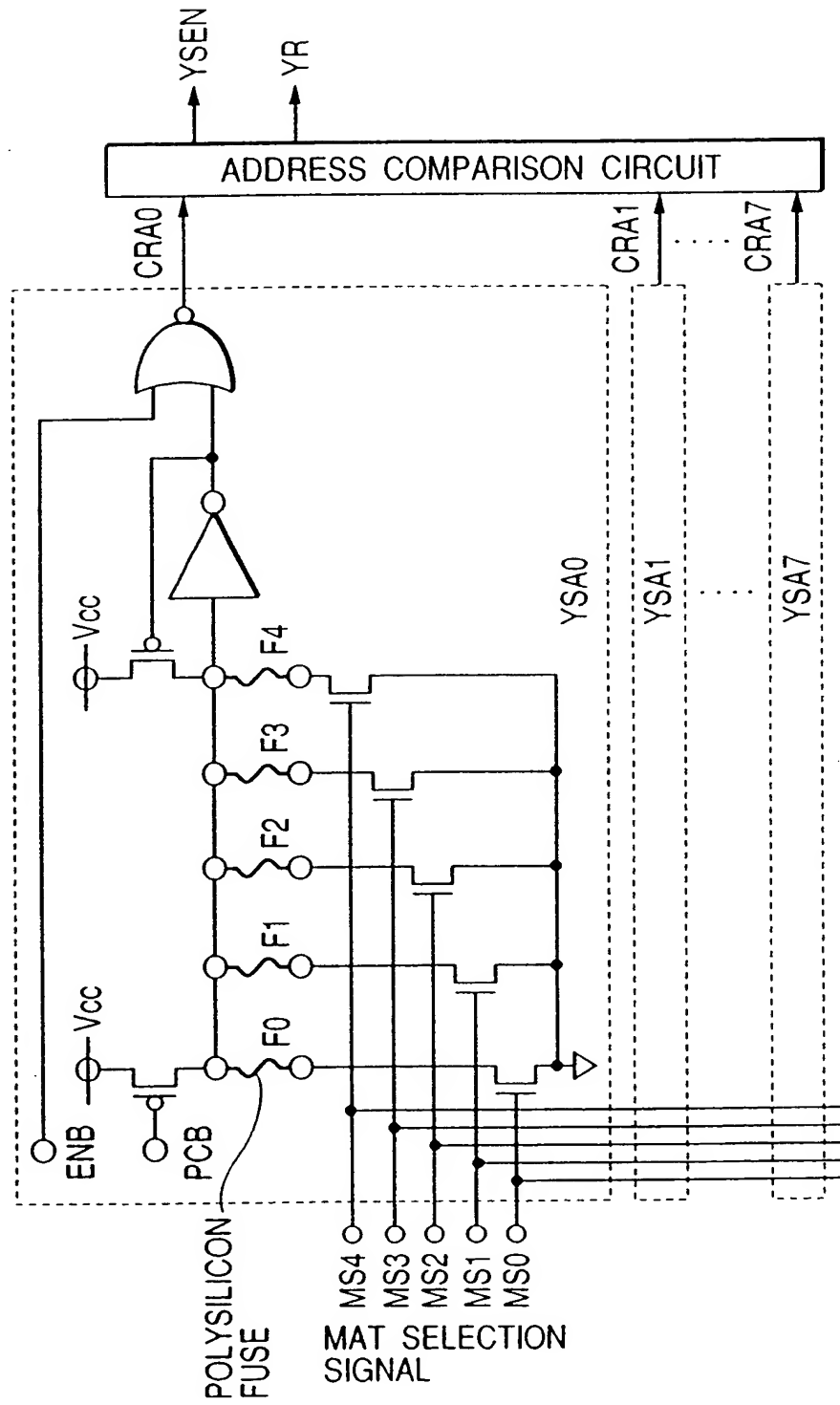


FIG. 13

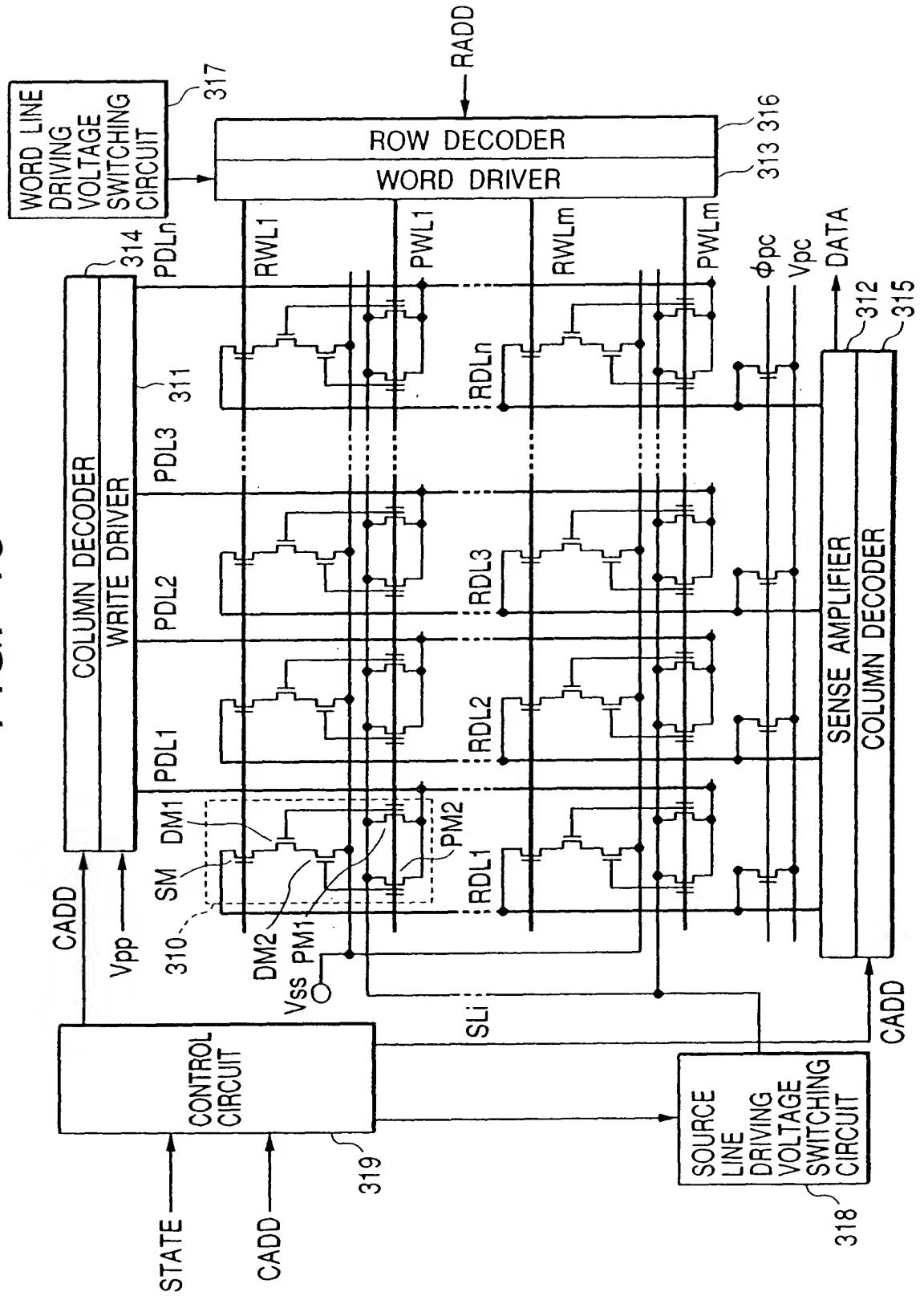
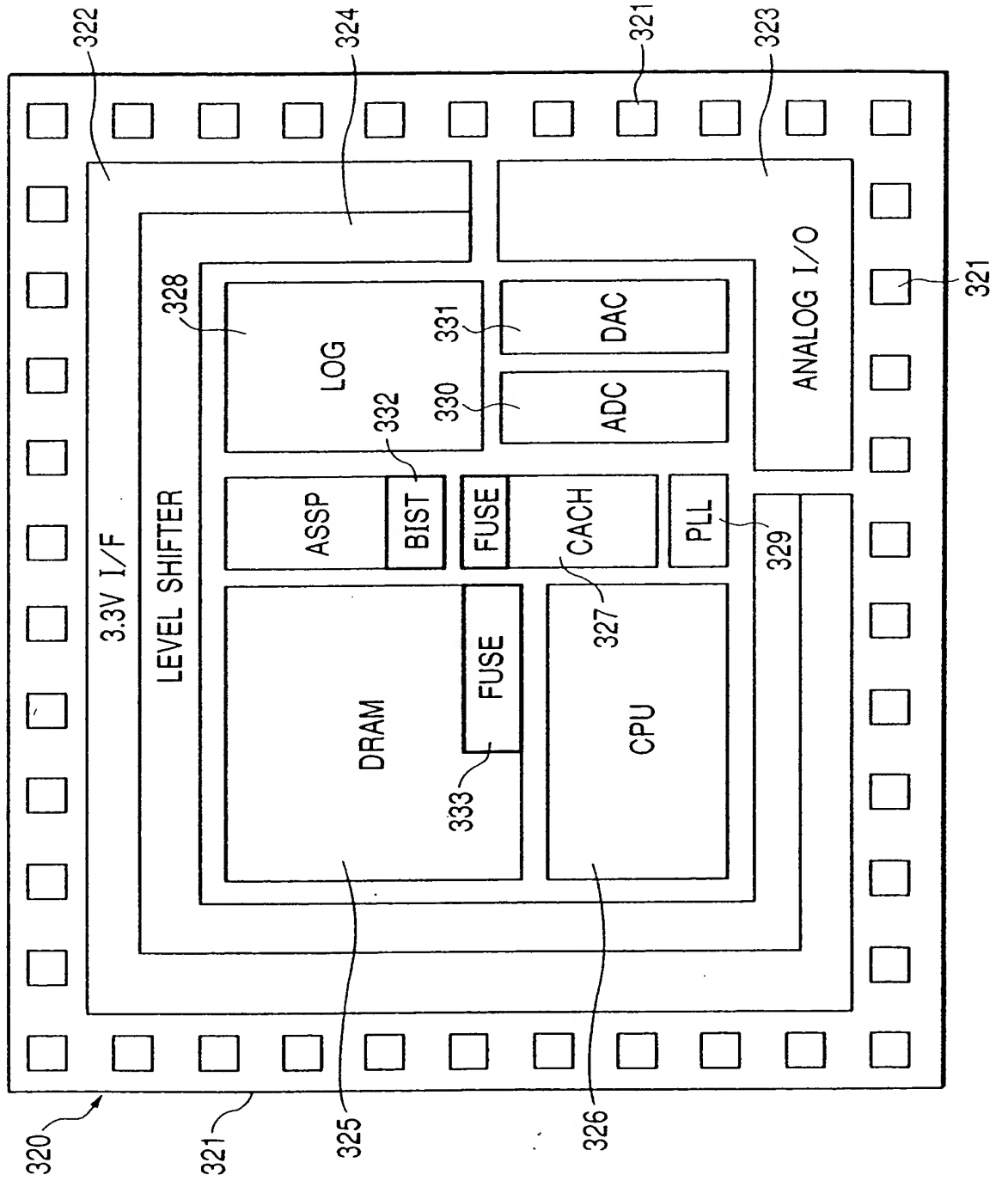


FIG. 14



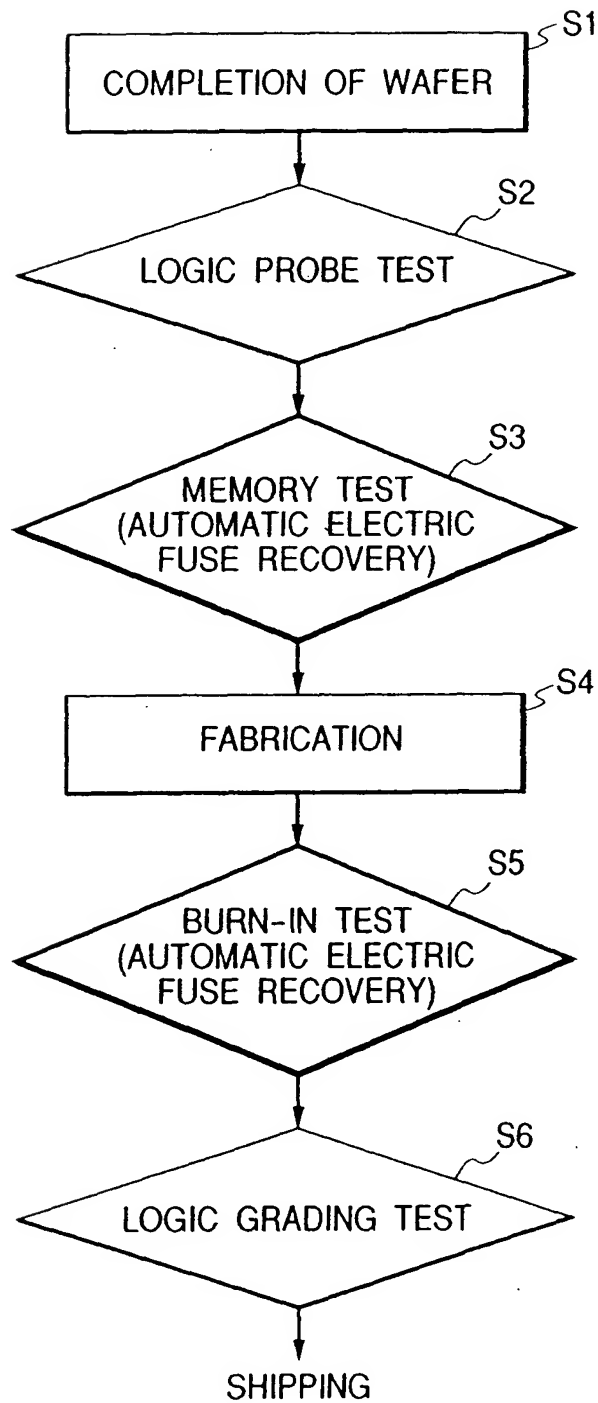
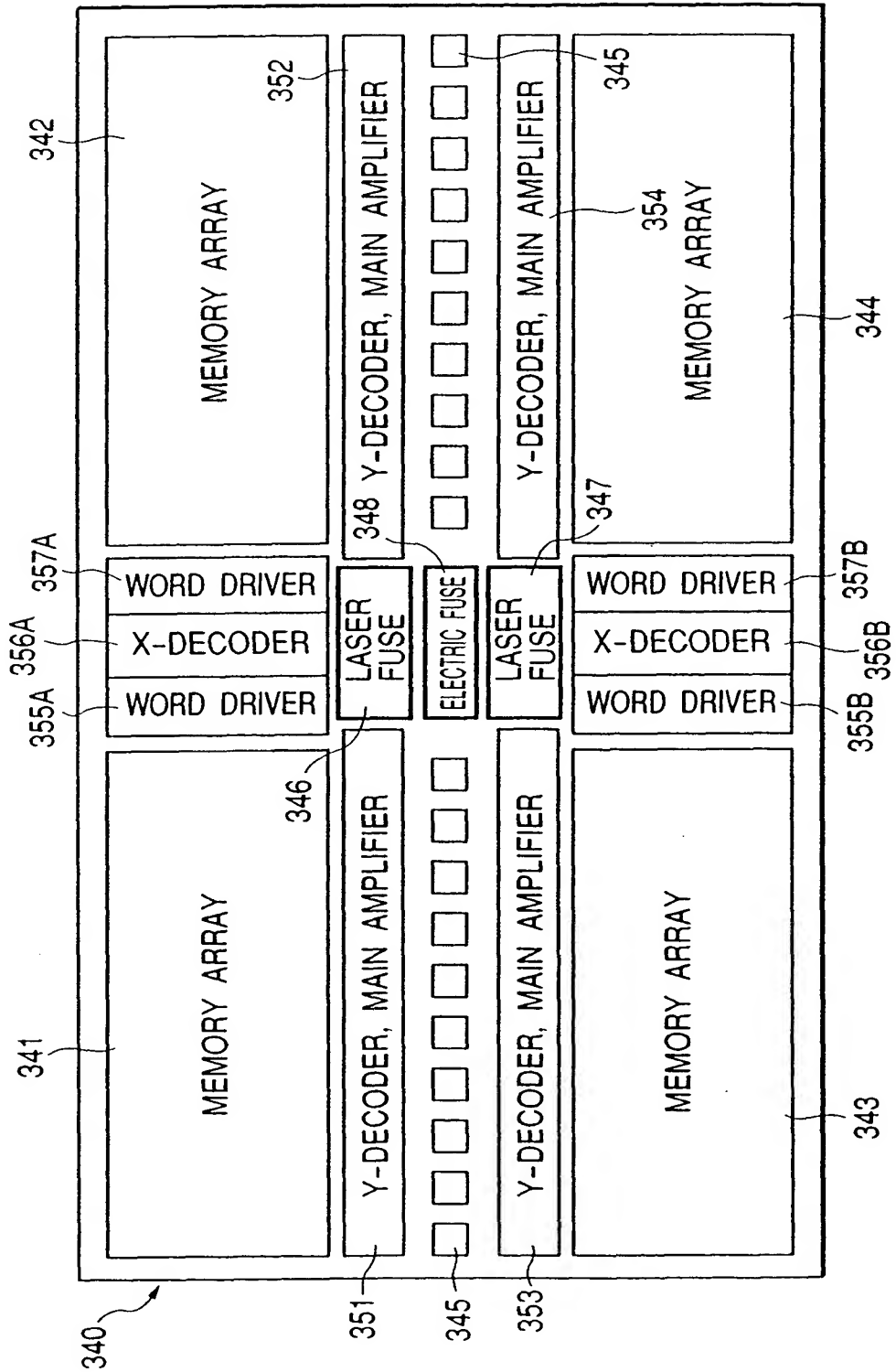
*FIG. 15*

FIG. 16



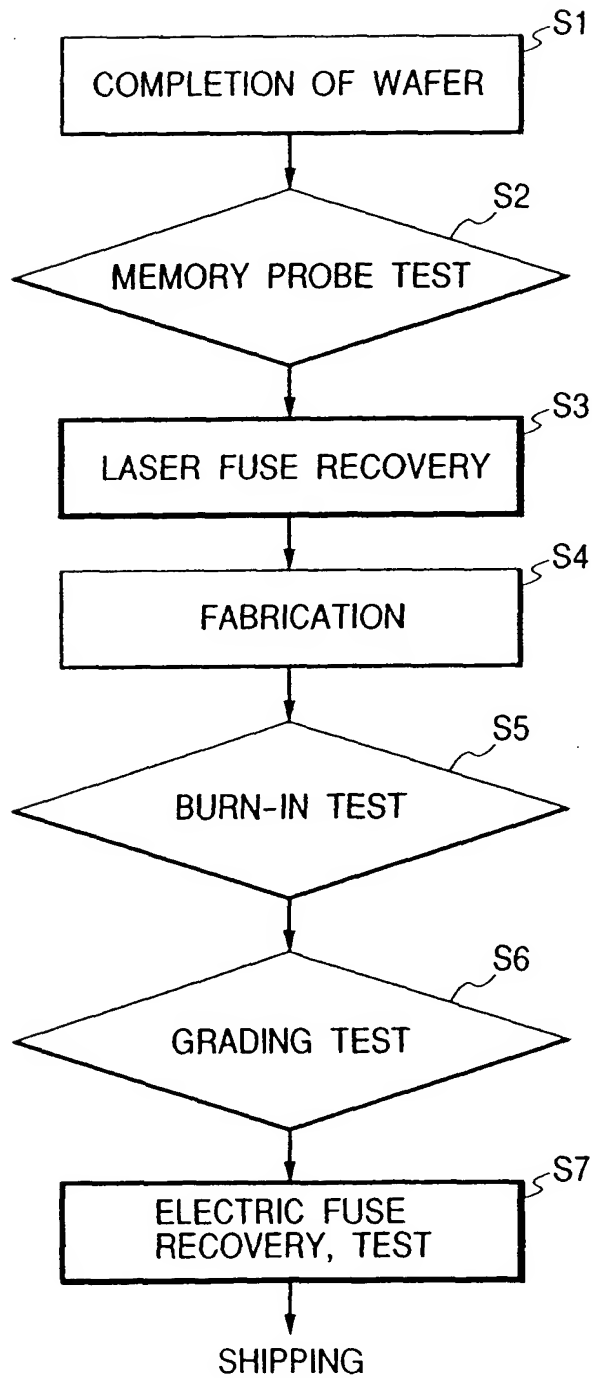
*FIG. 17*

FIG. 18

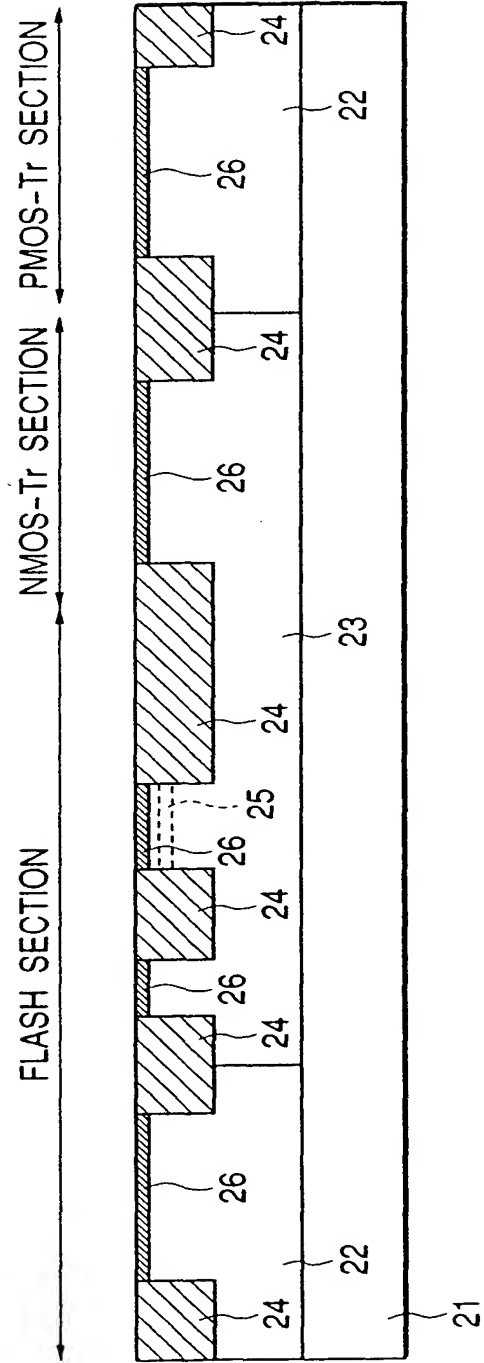




FIG. 19

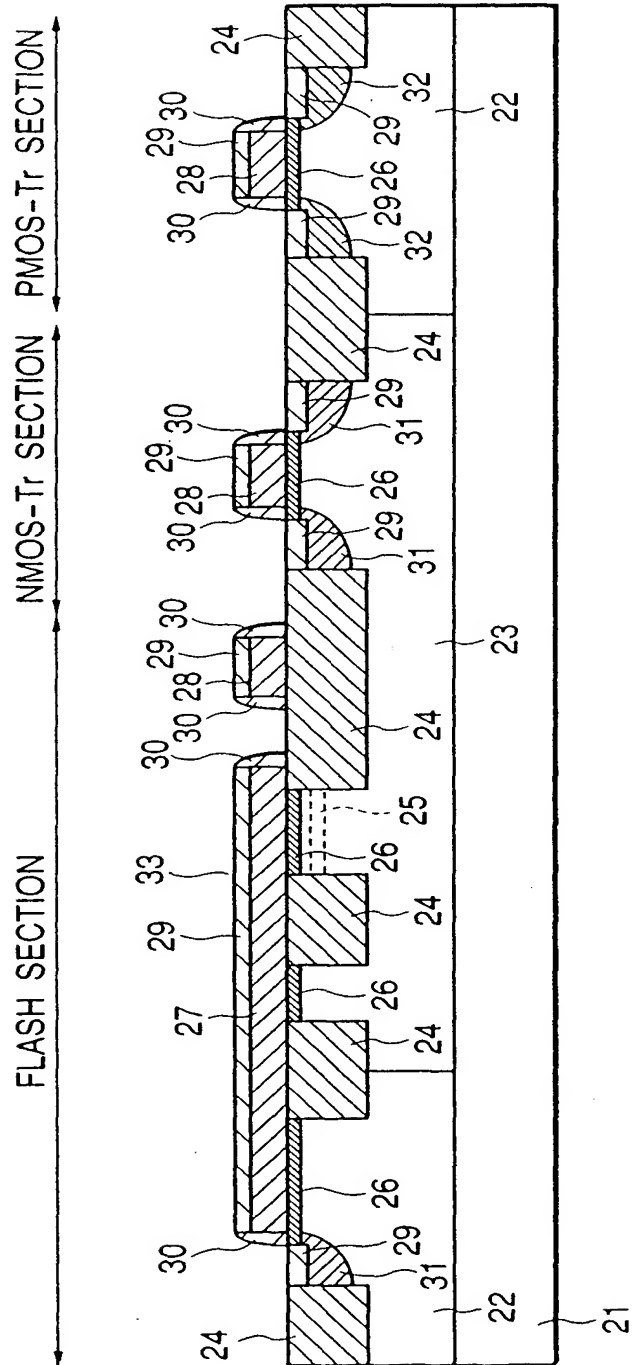


FIG. 20

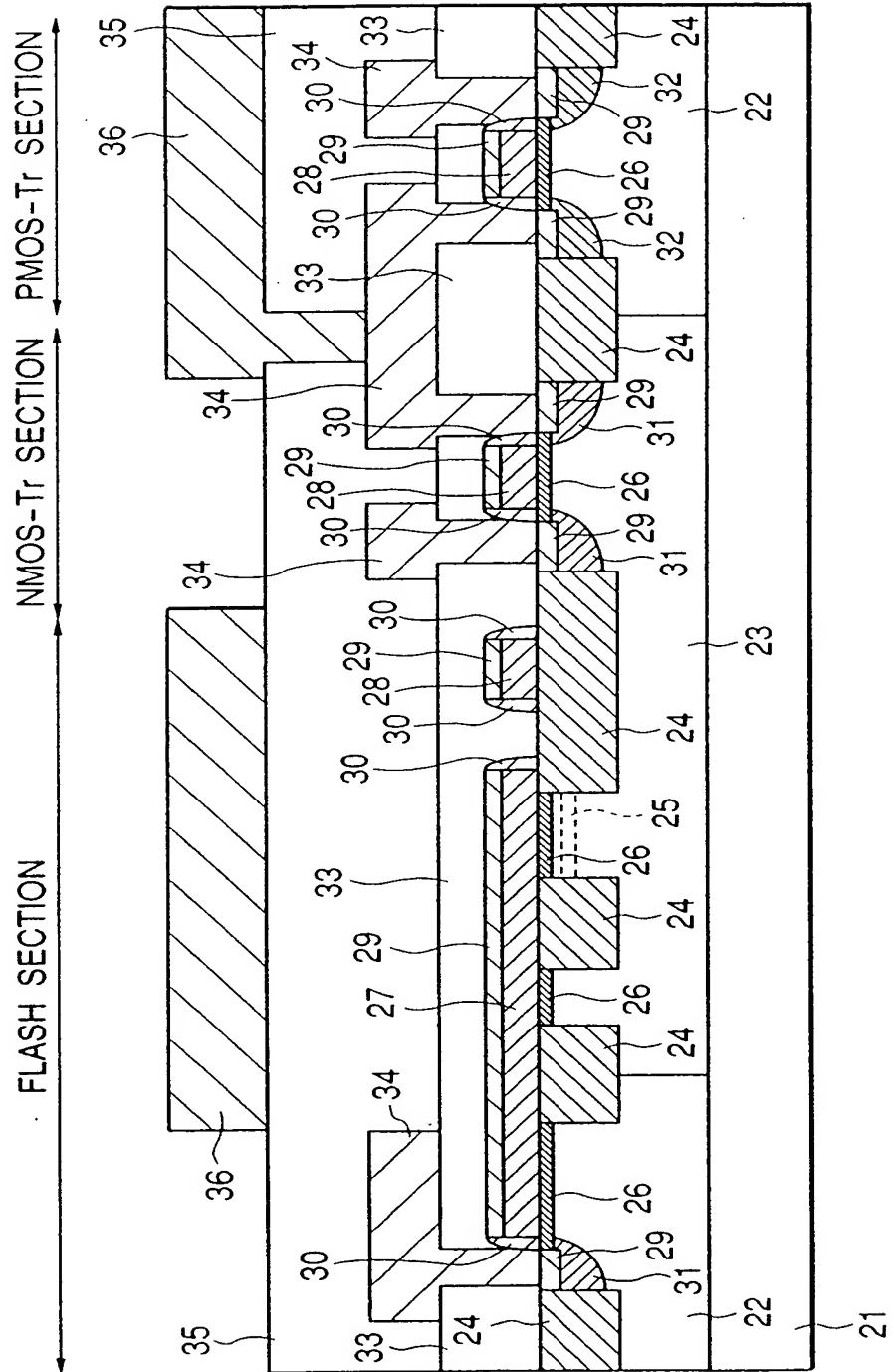
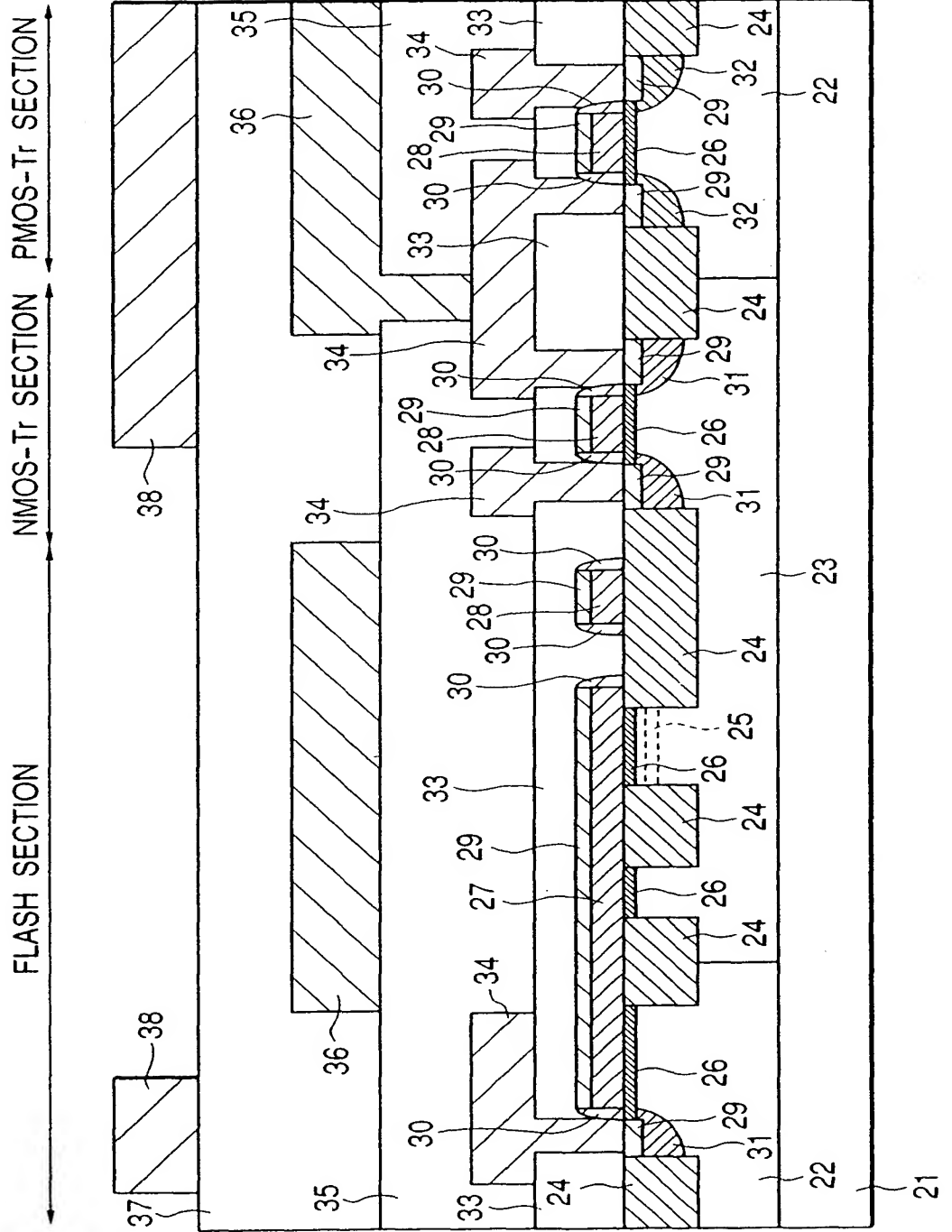


FIG. 21



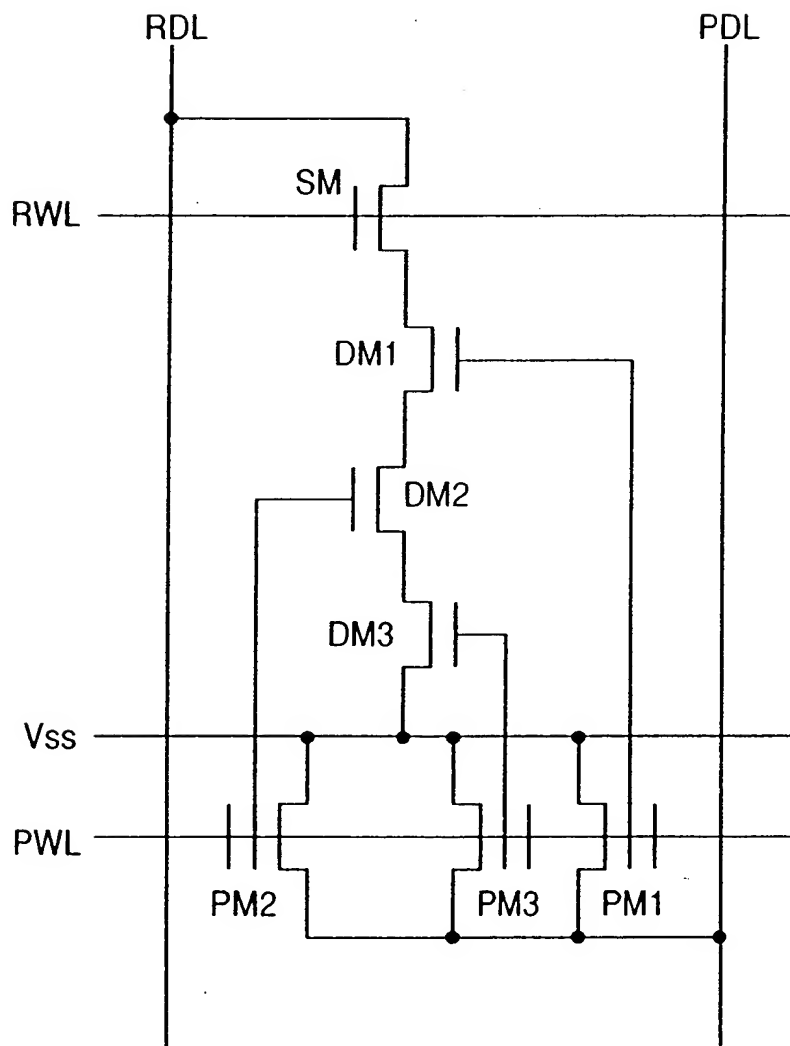
*FIG. 22*

FIG. 24

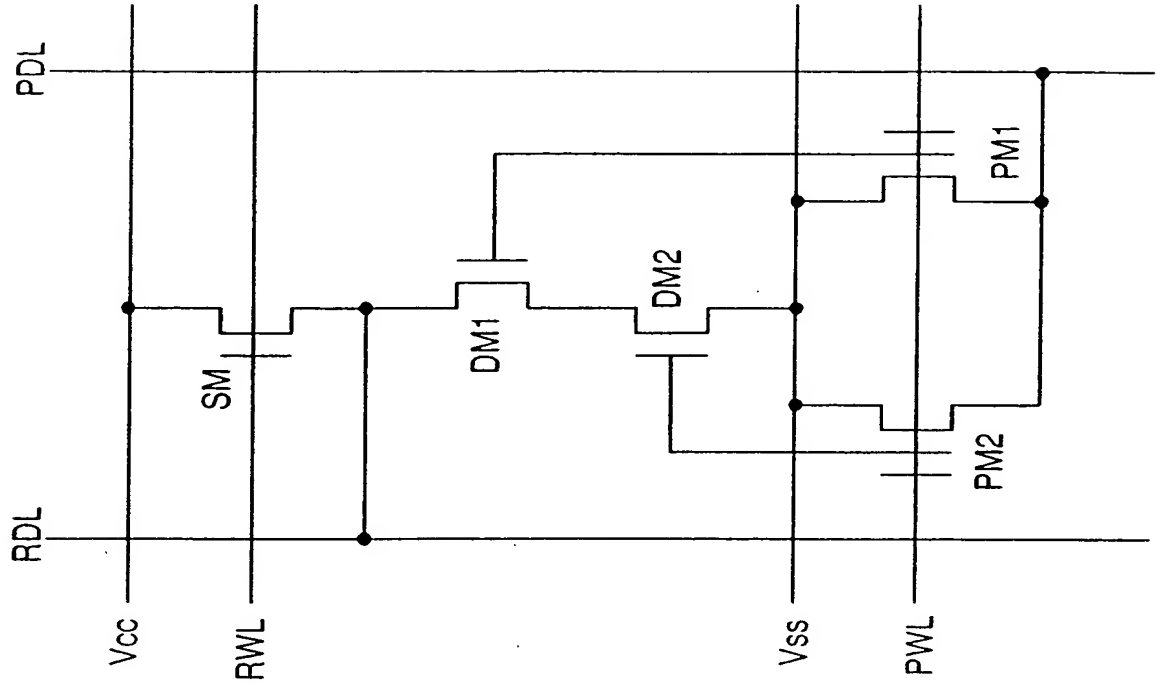
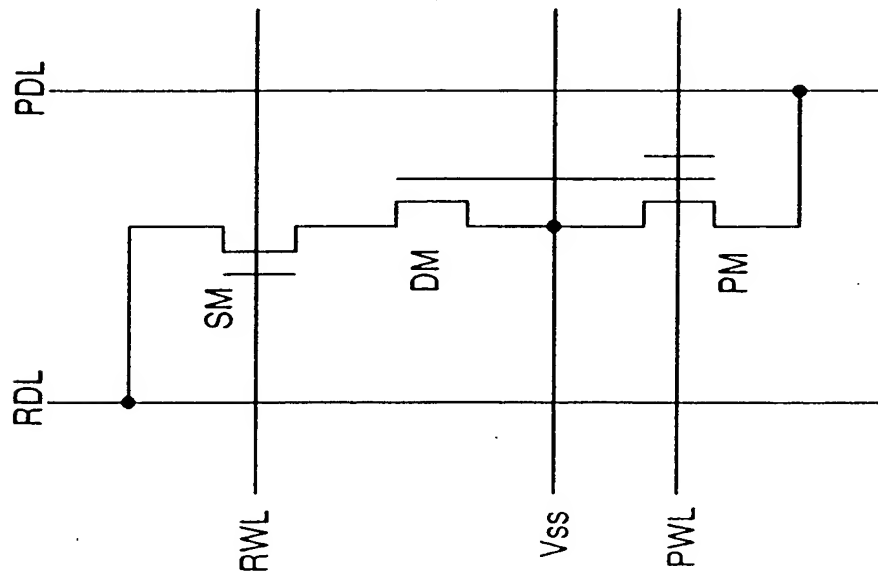


FIG. 23



*FIG. 25*

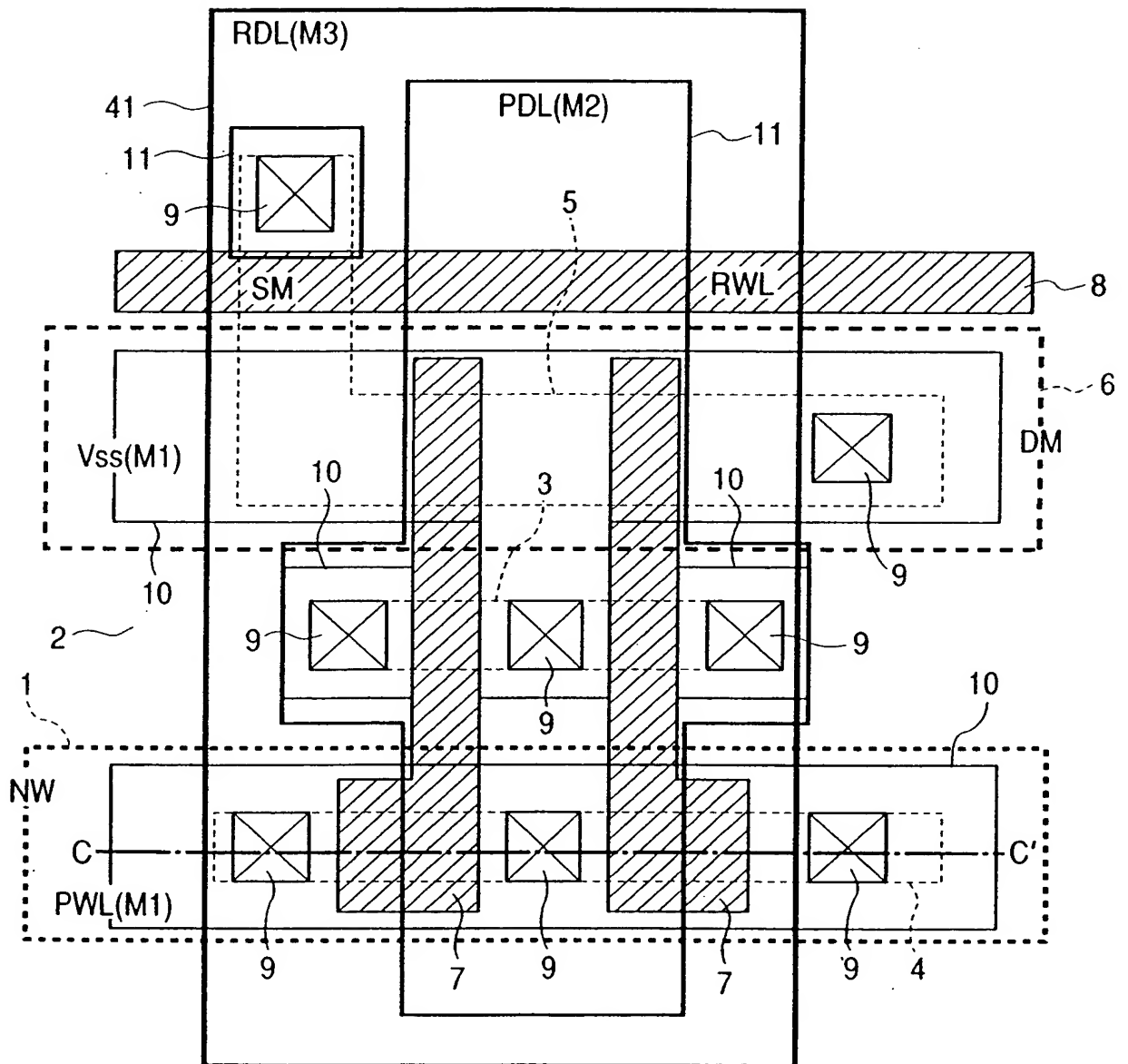


FIG. 26

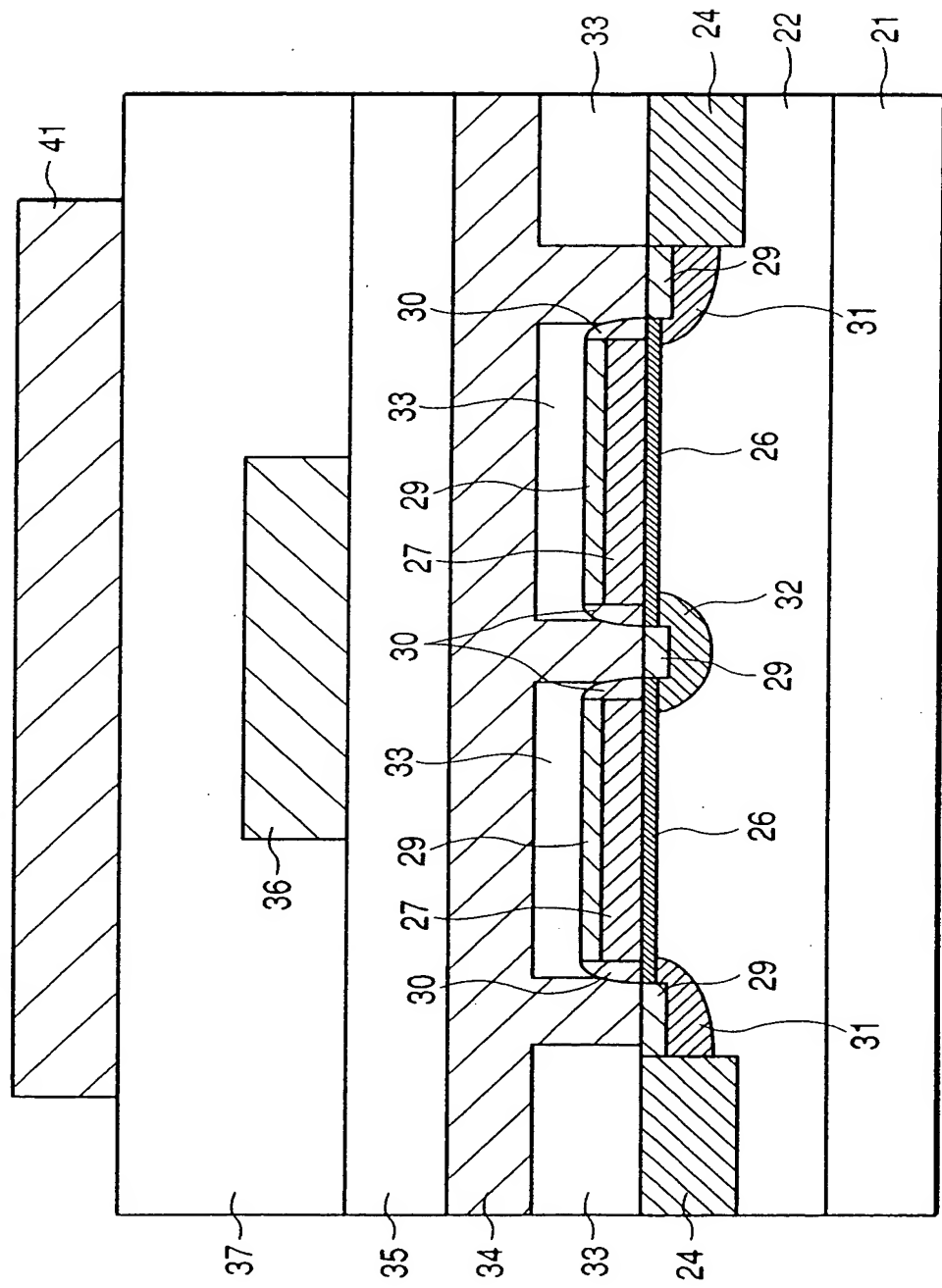


FIG. 27

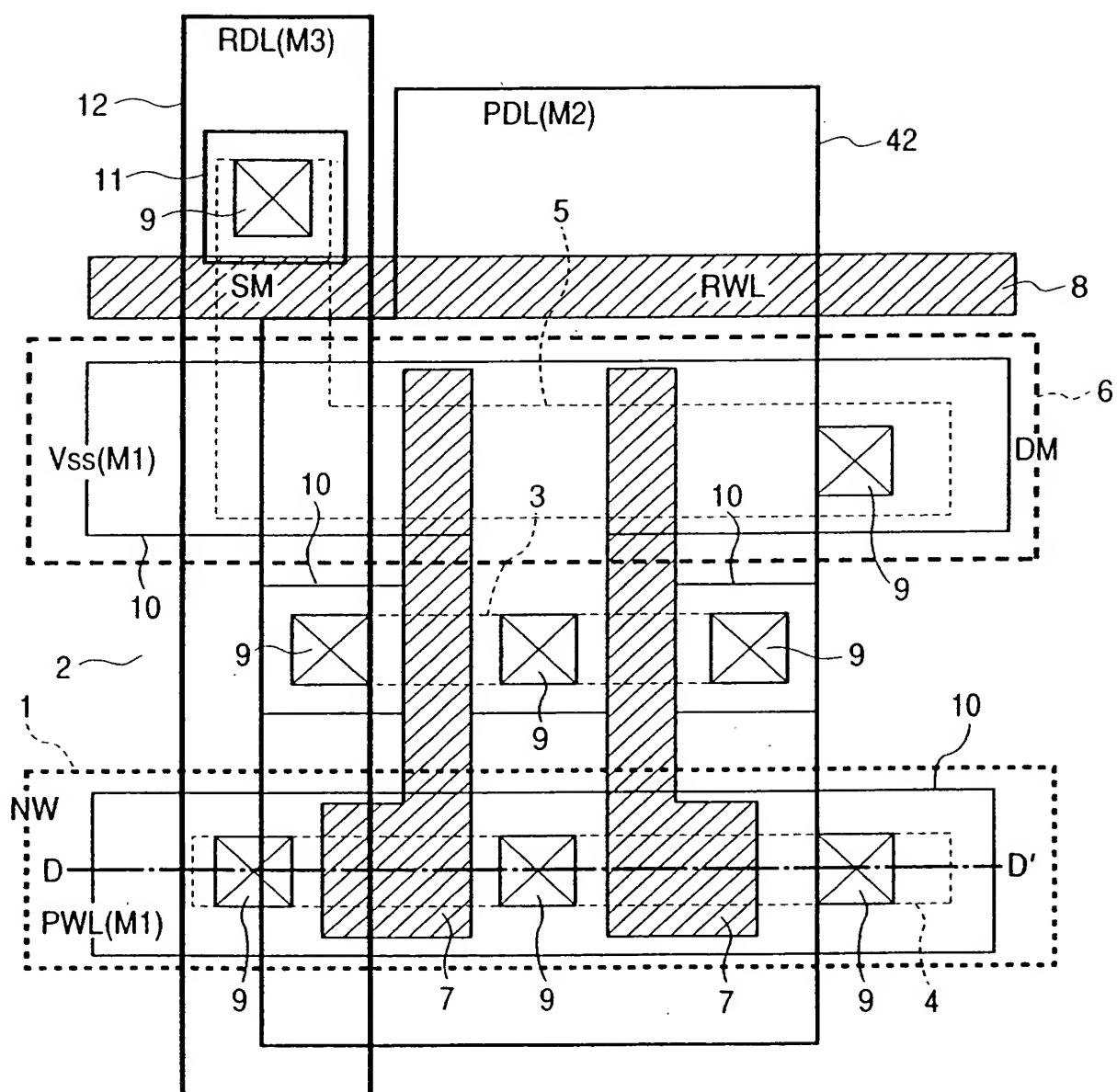




FIG. 28

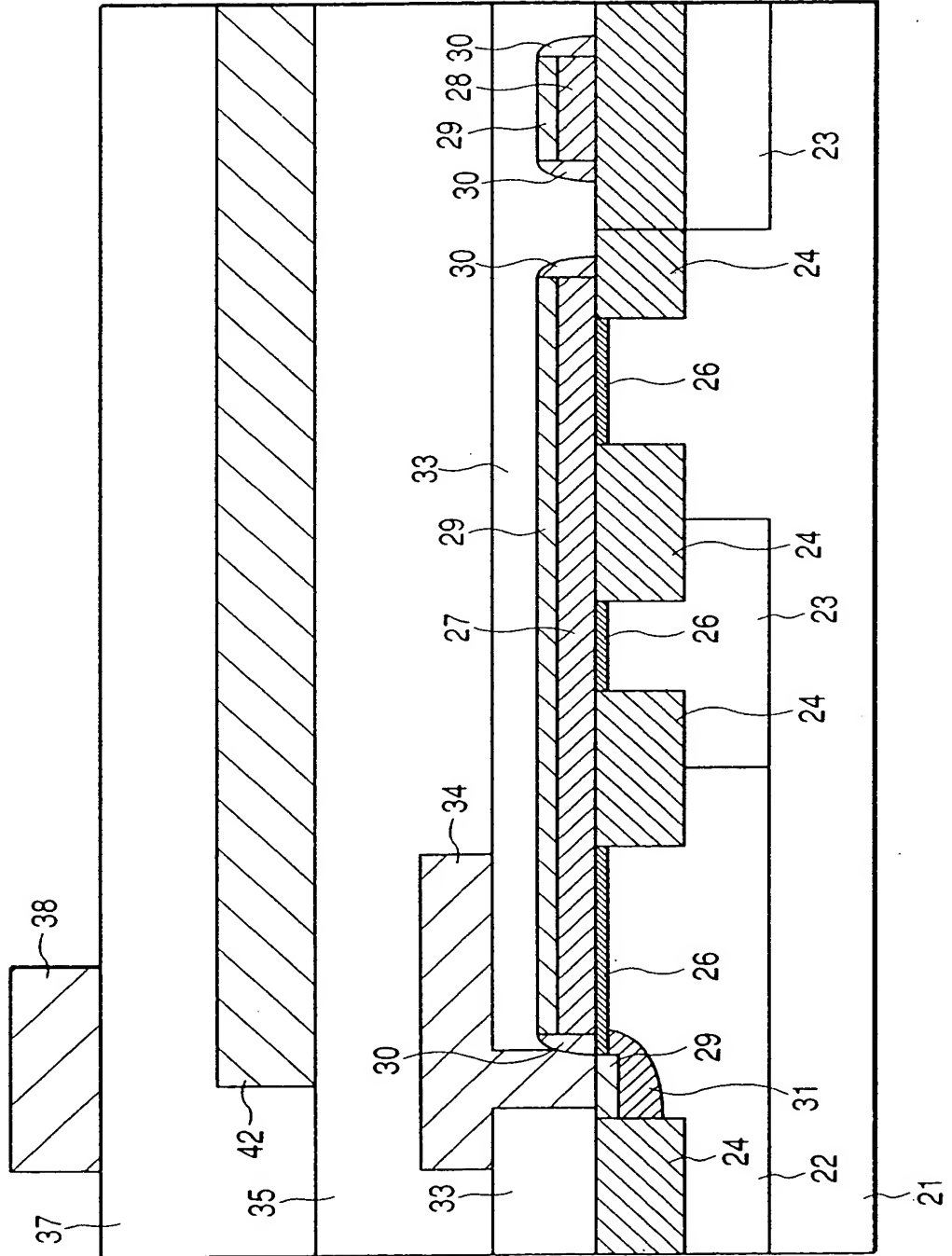


FIG. 29

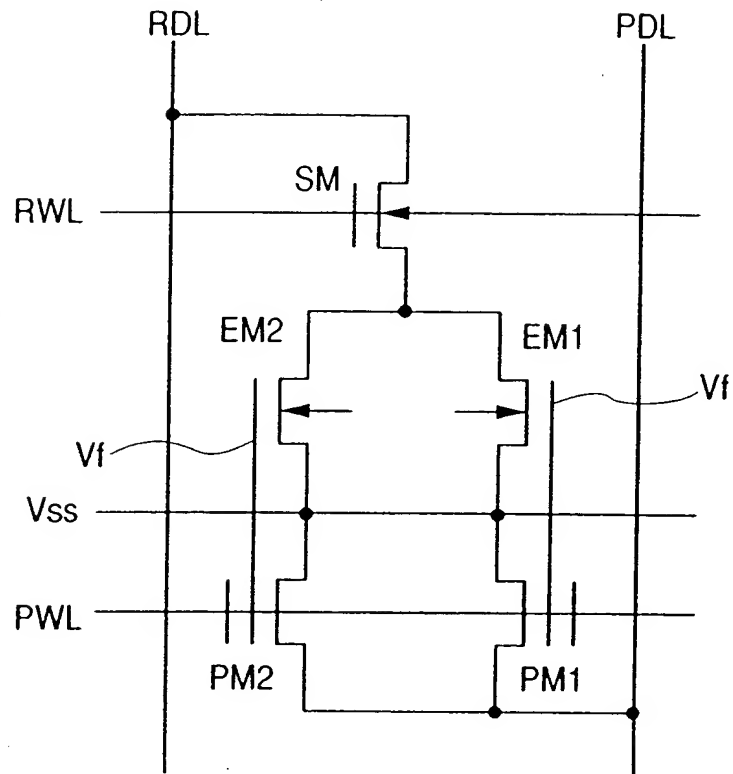


FIG. 30

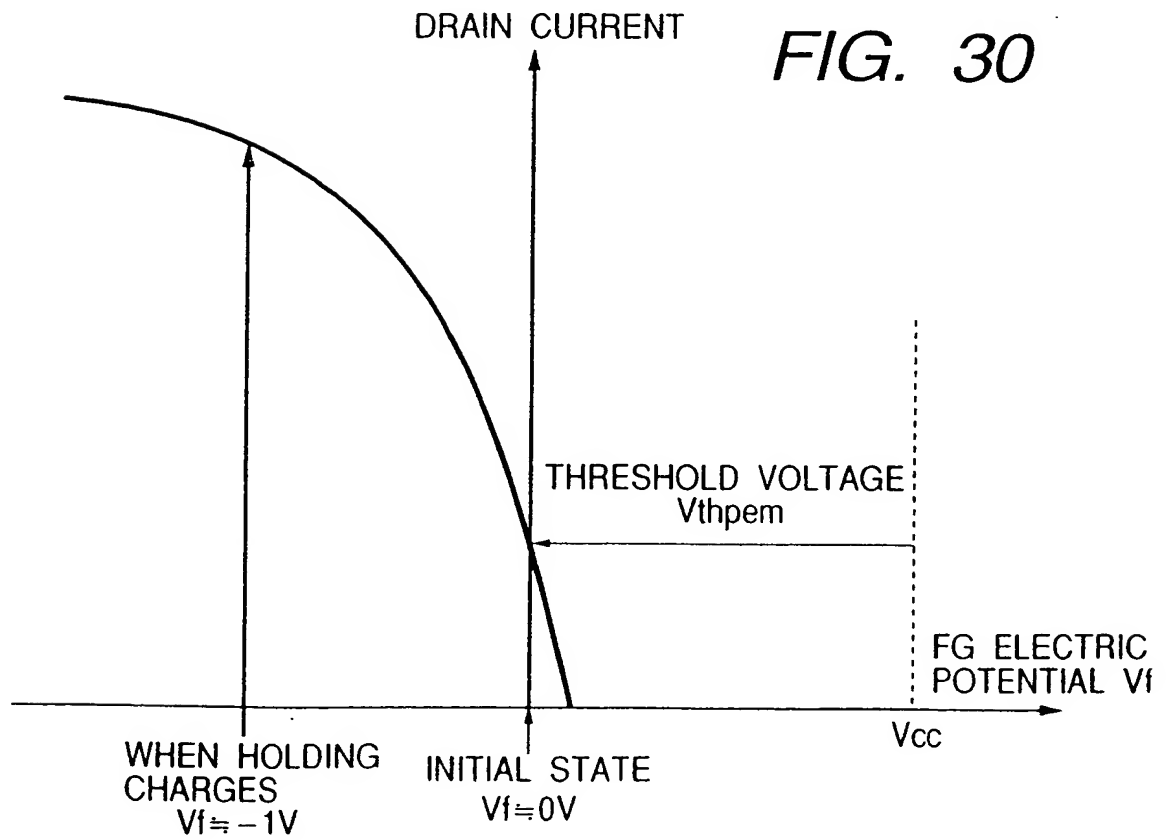
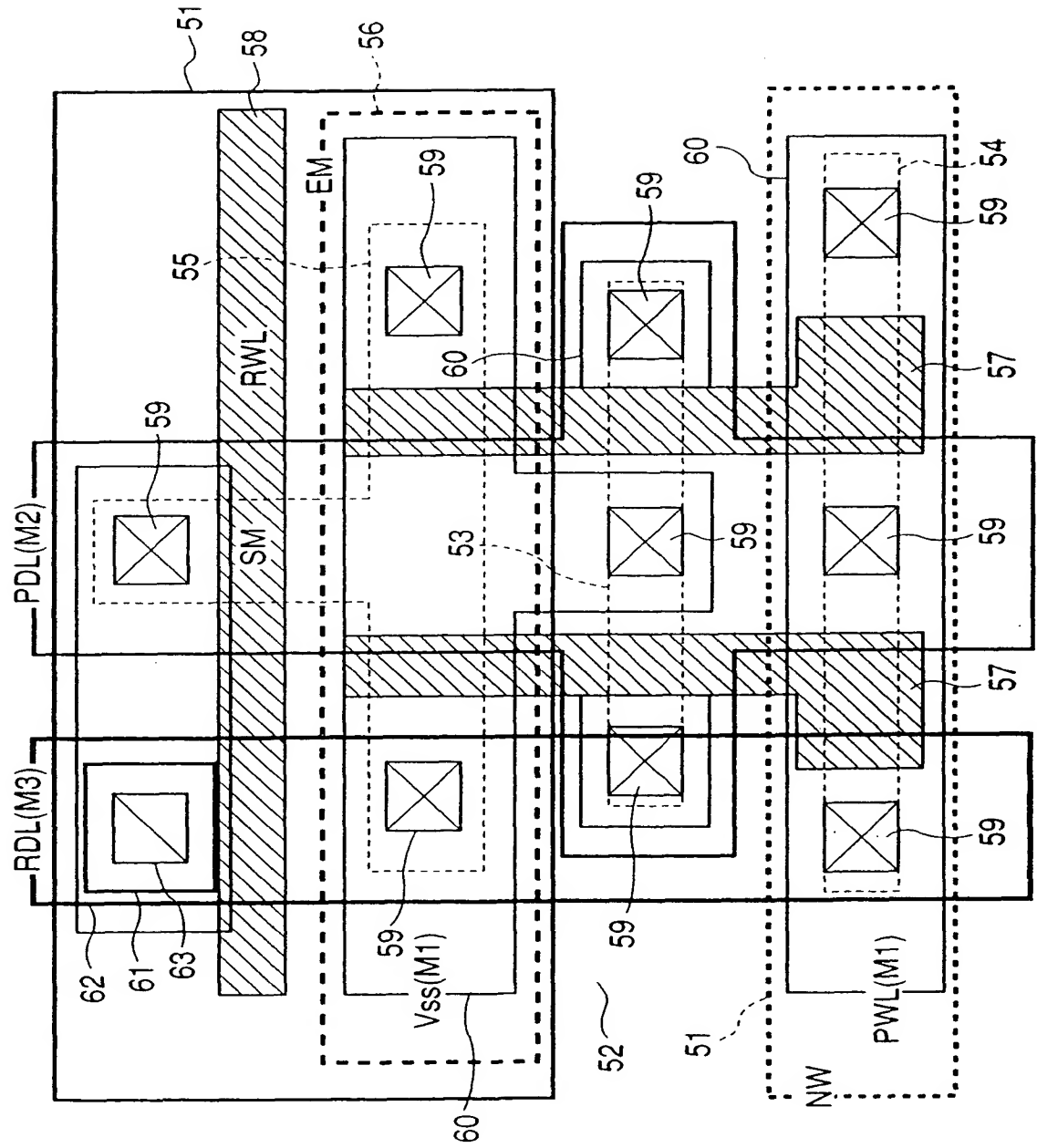


FIG. 31



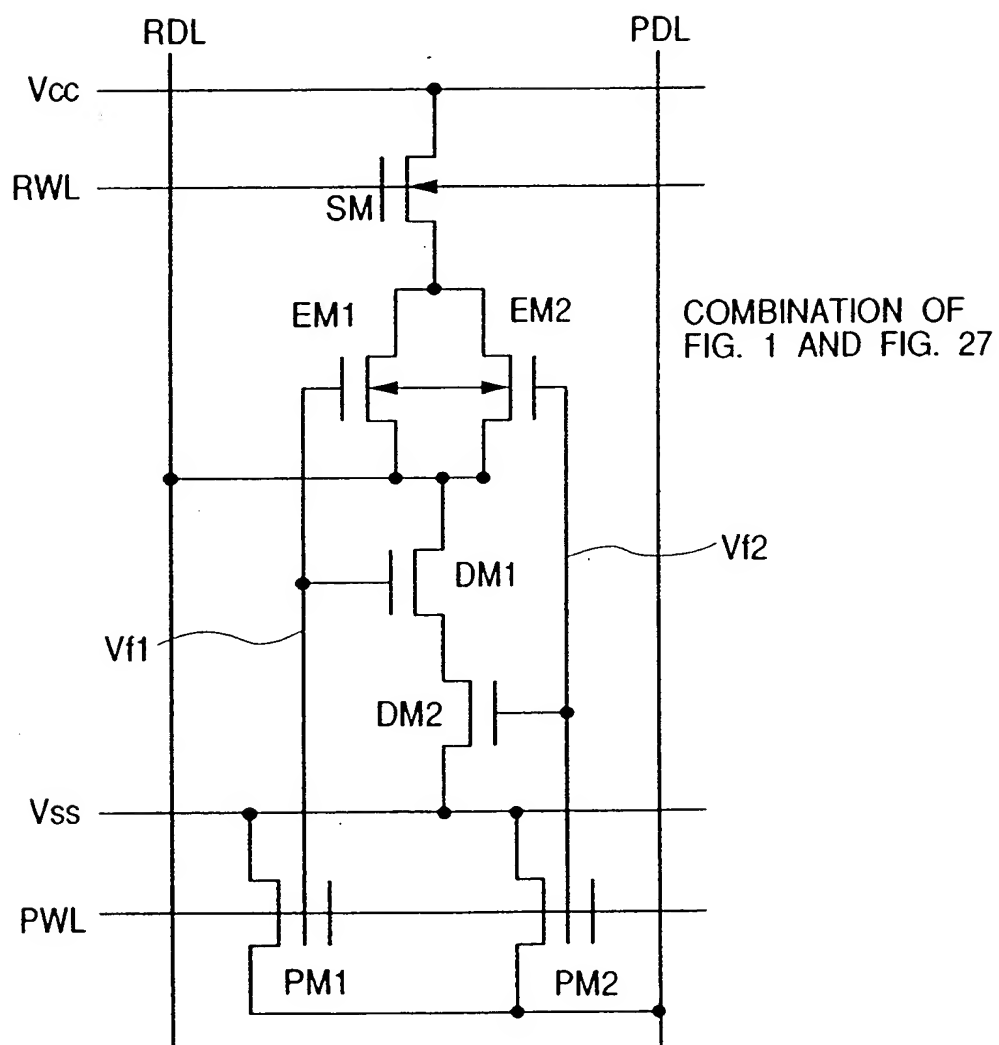
*FIG. 32*

FIG. 33

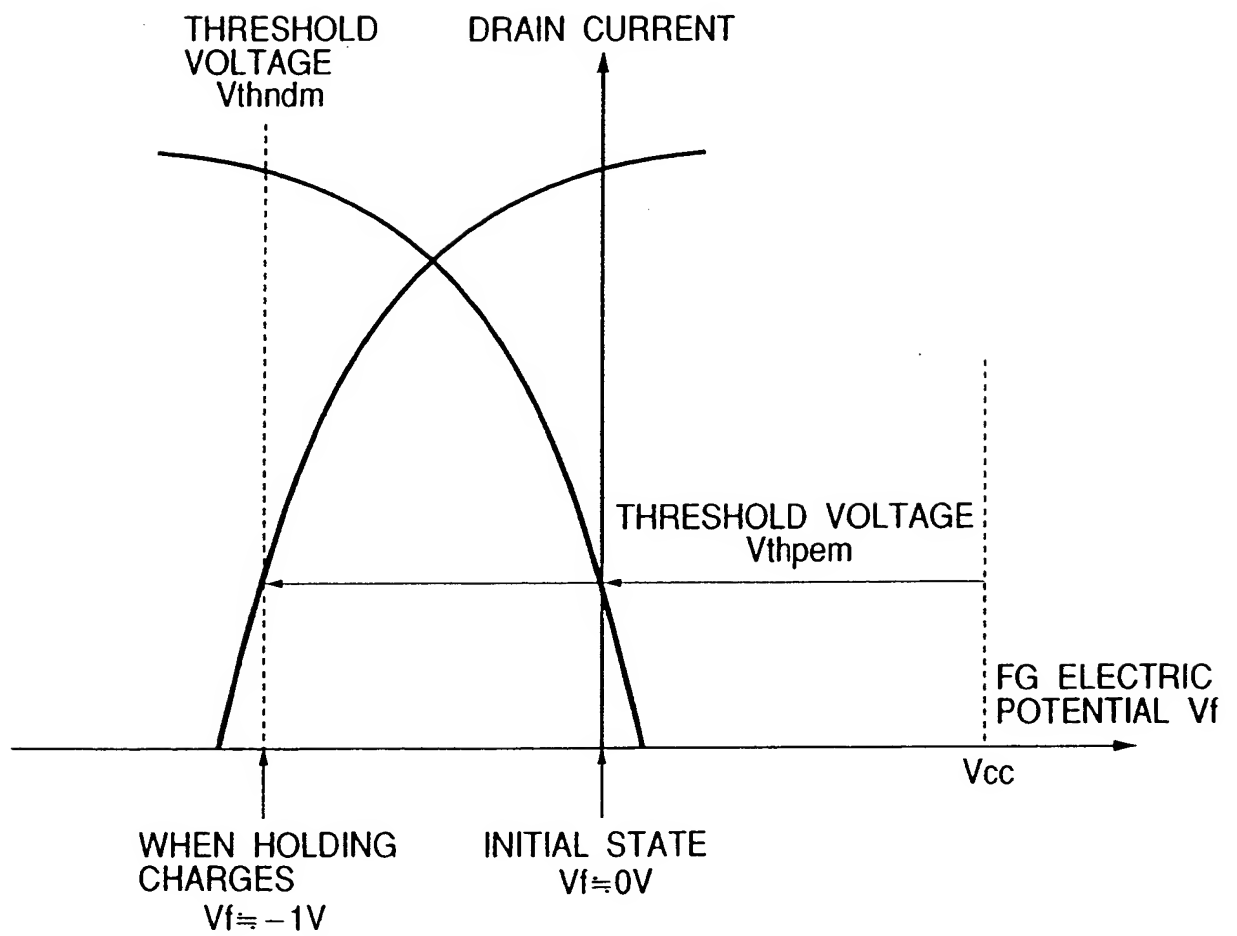
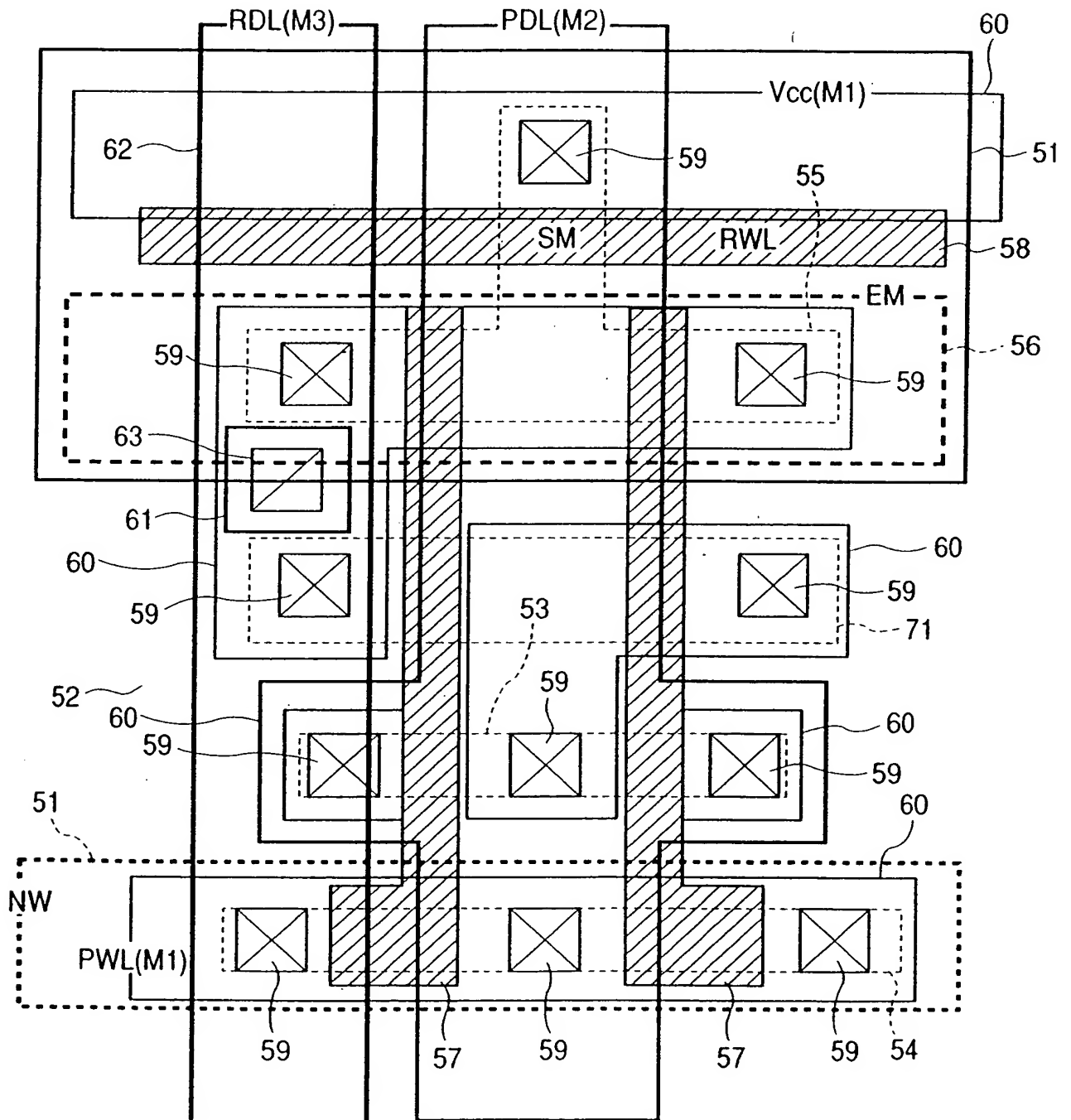


FIG. 34



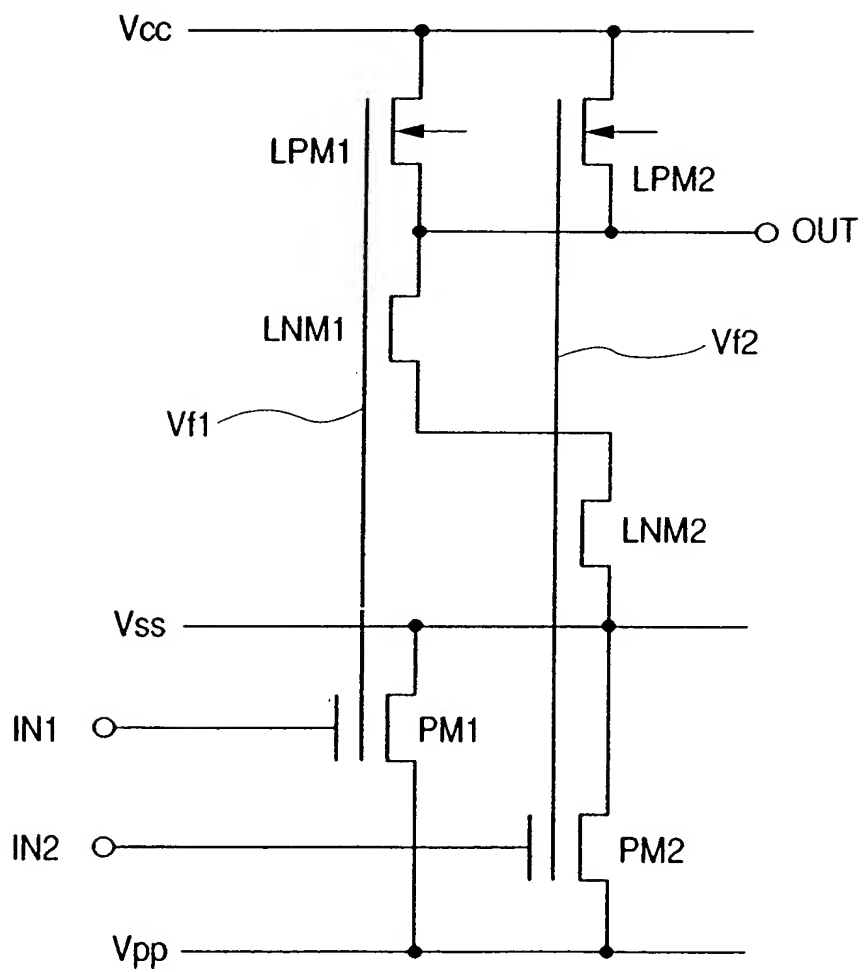
*FIG. 35*

FIG. 36

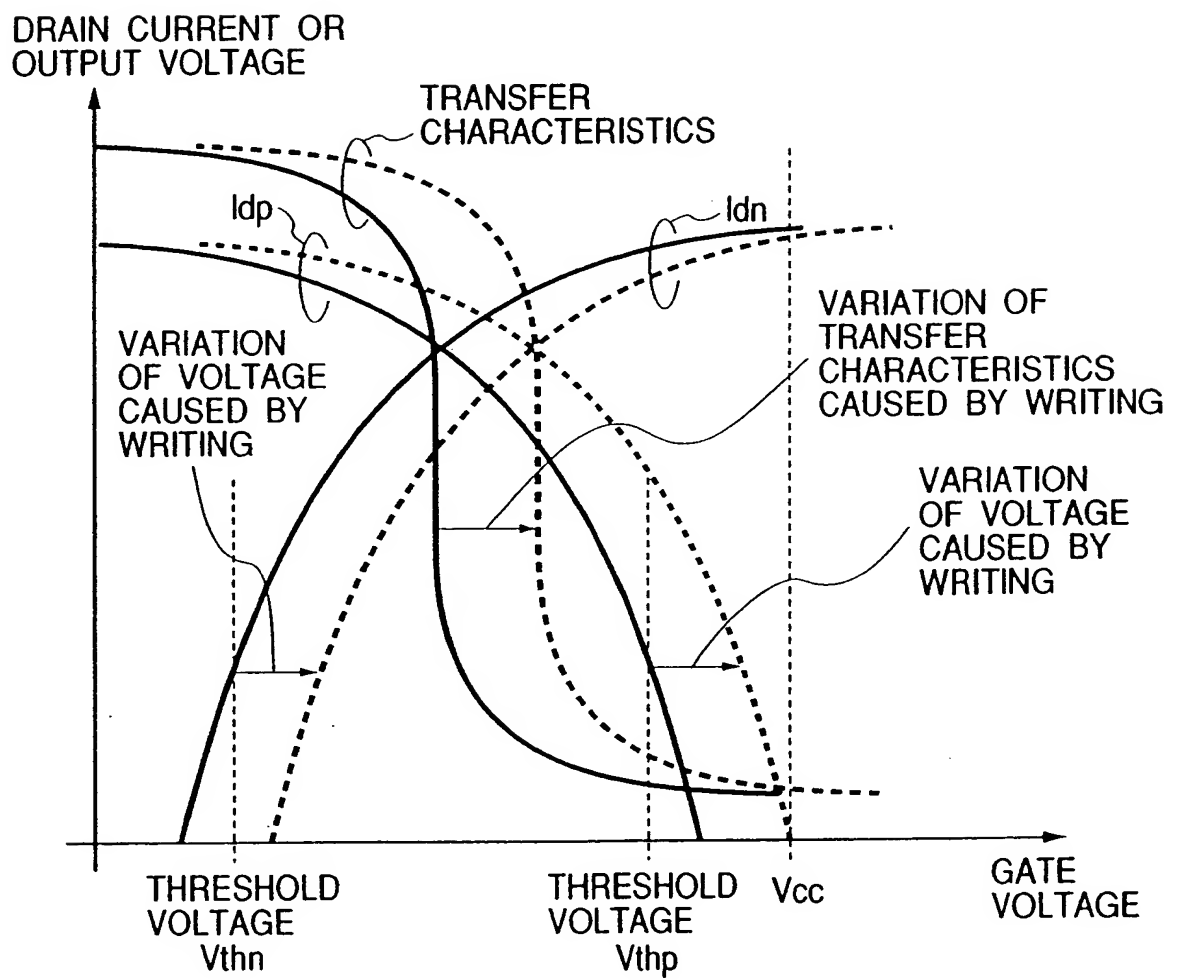
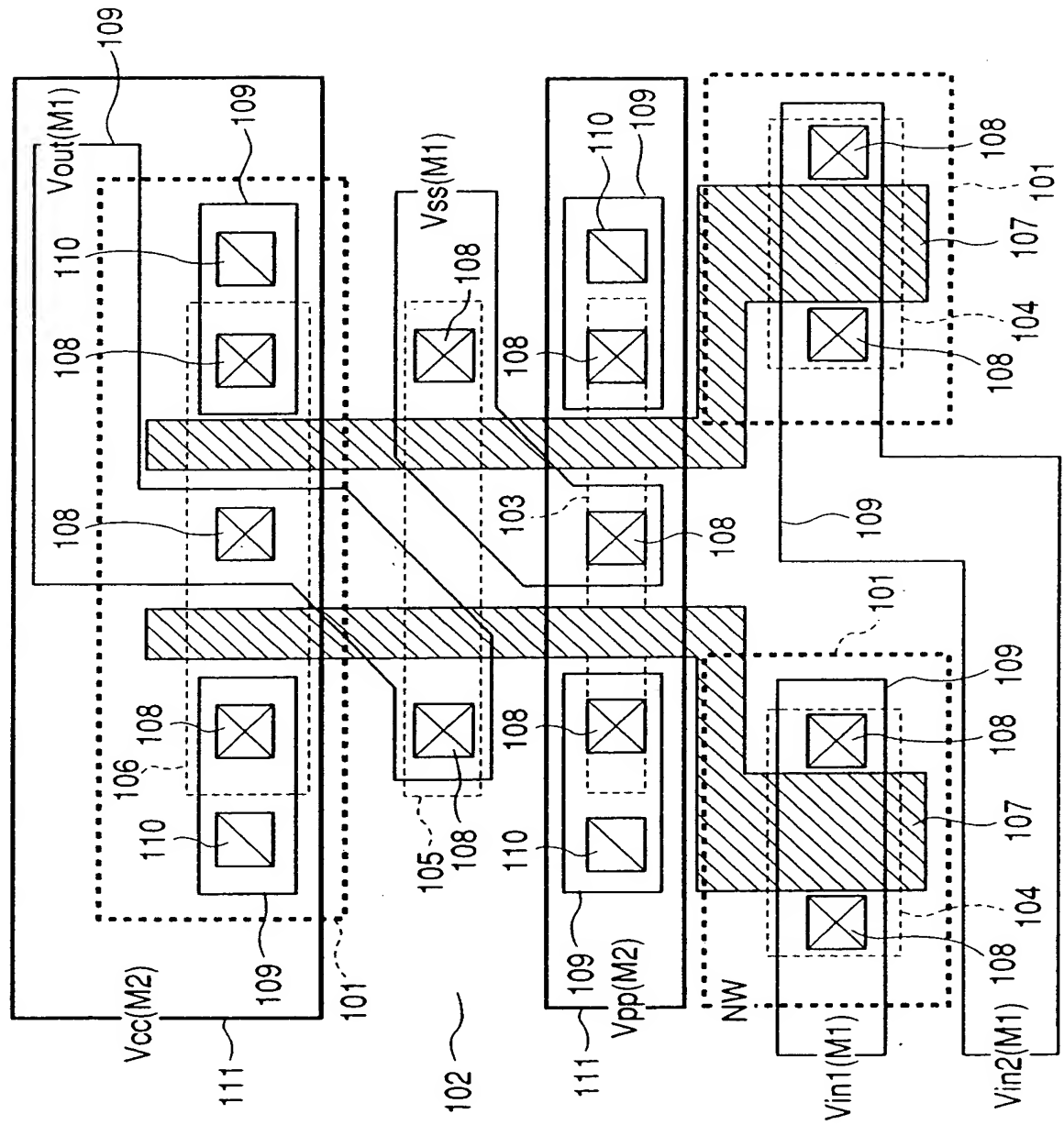
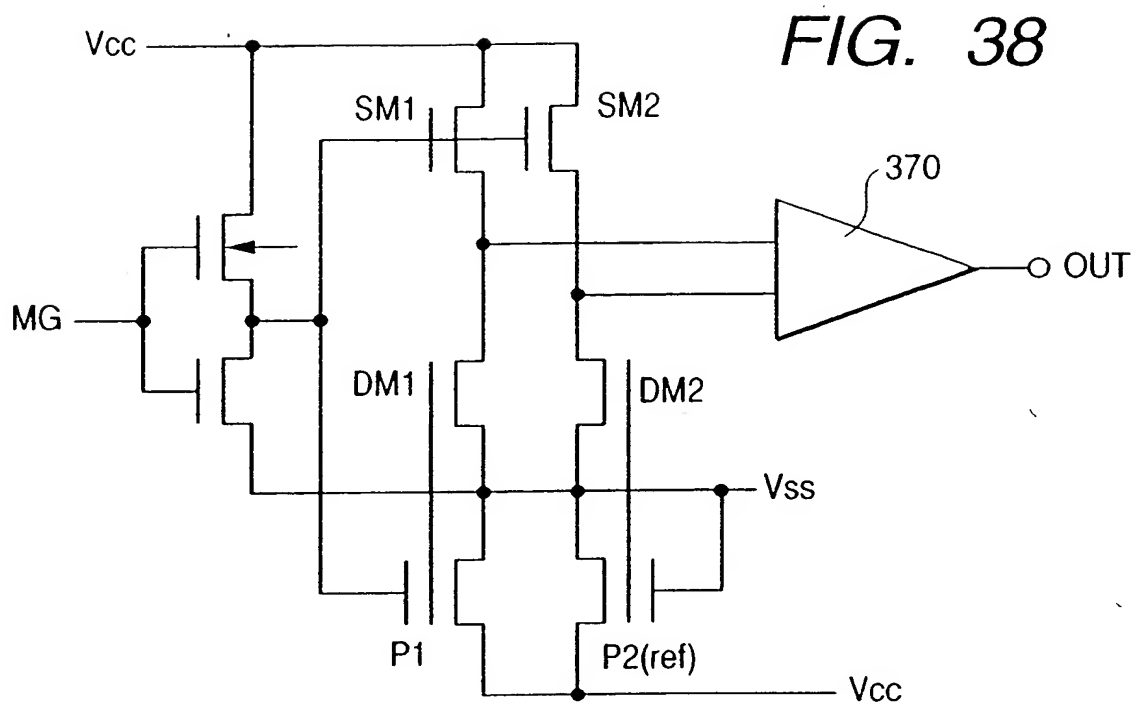




FIG. 37





**FIG. 39**

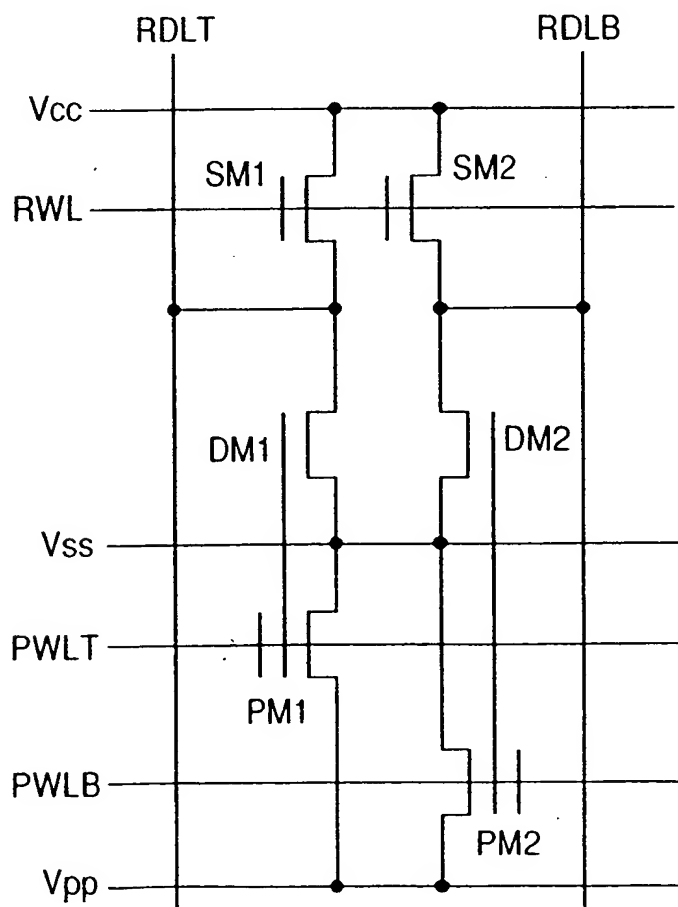
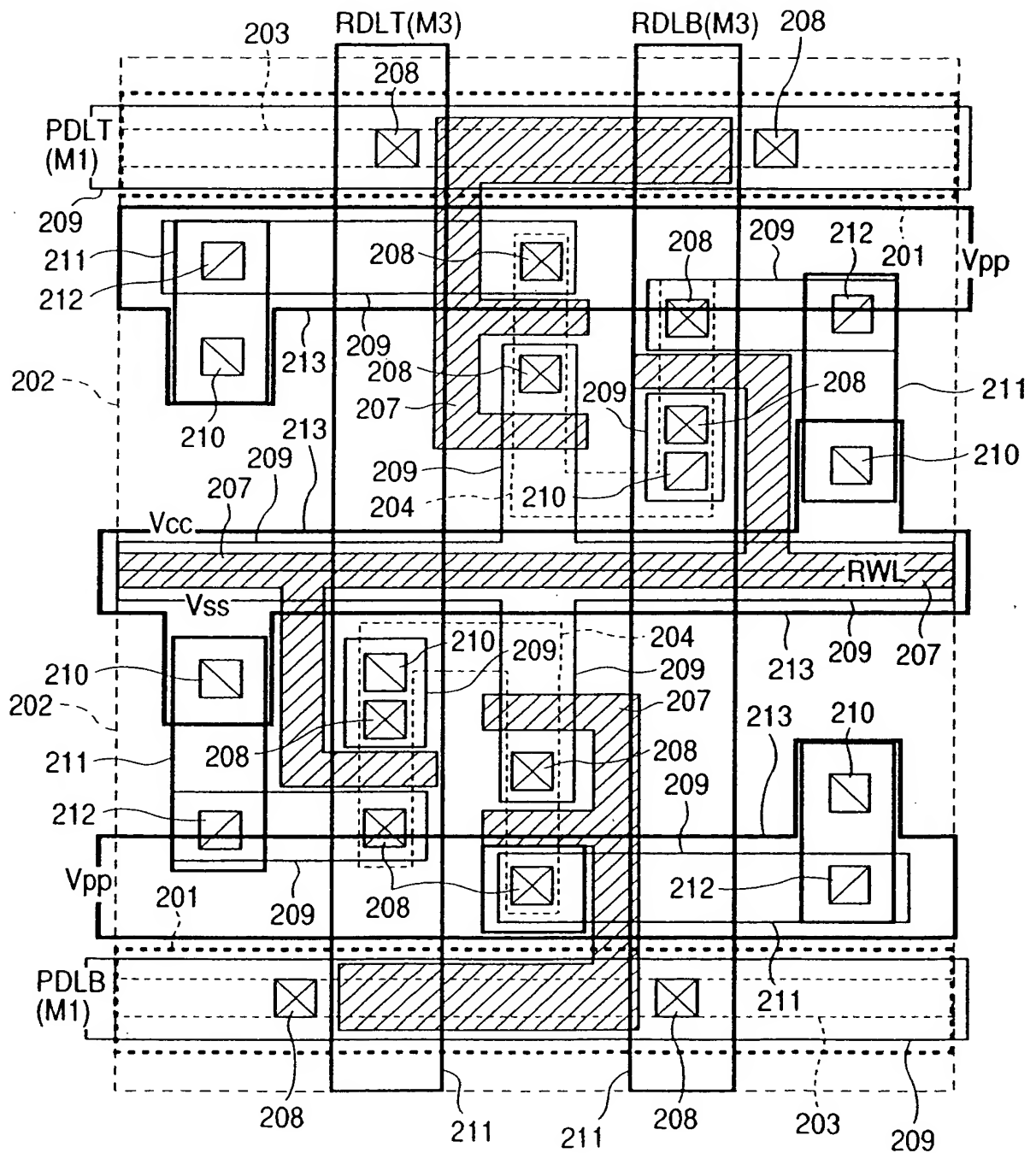


FIG. 40



**FIG. 41**

35 BIT FUSE MODULE BLOCK DIAGRAM

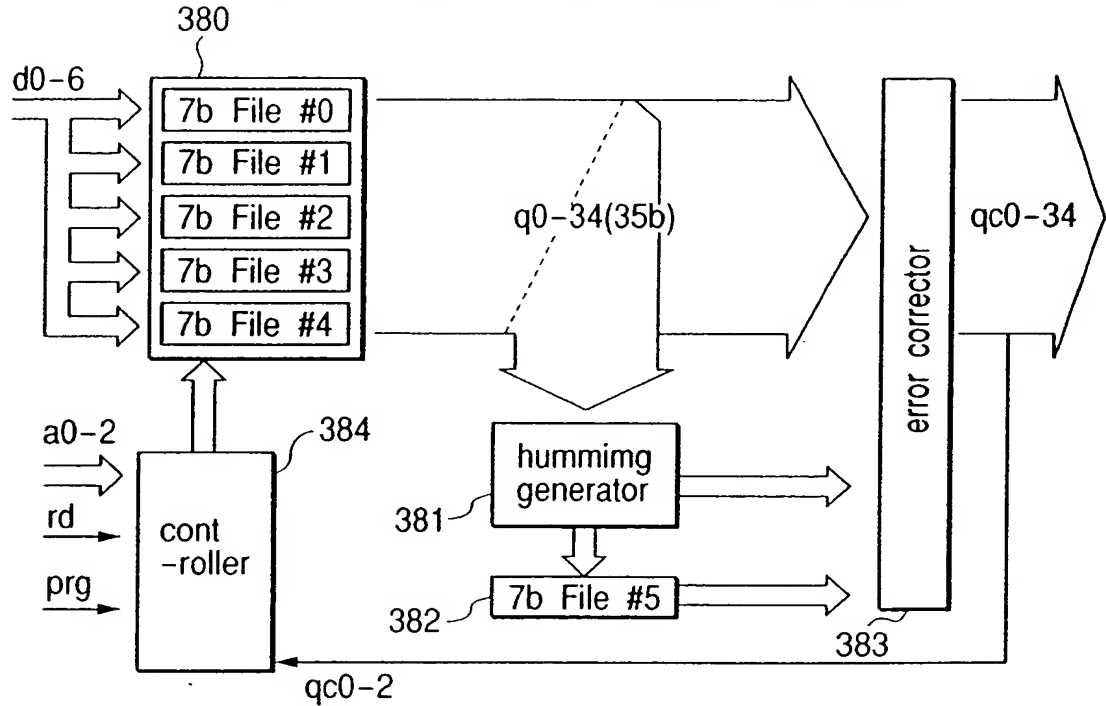
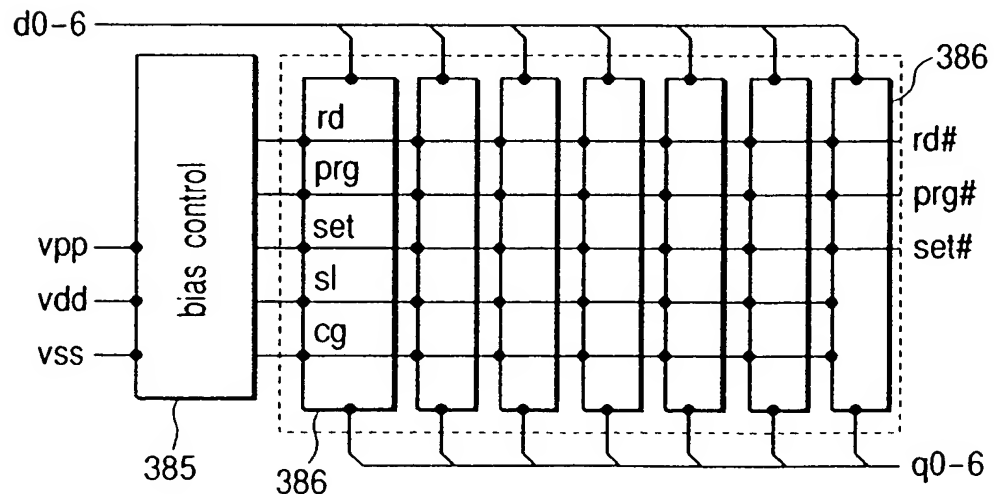

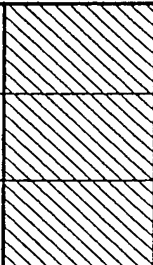
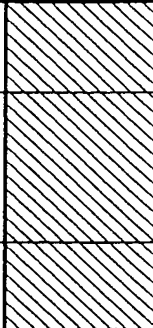
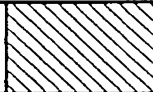
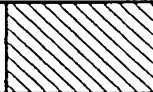
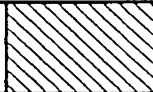
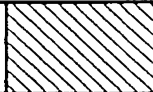
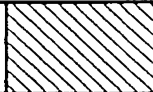
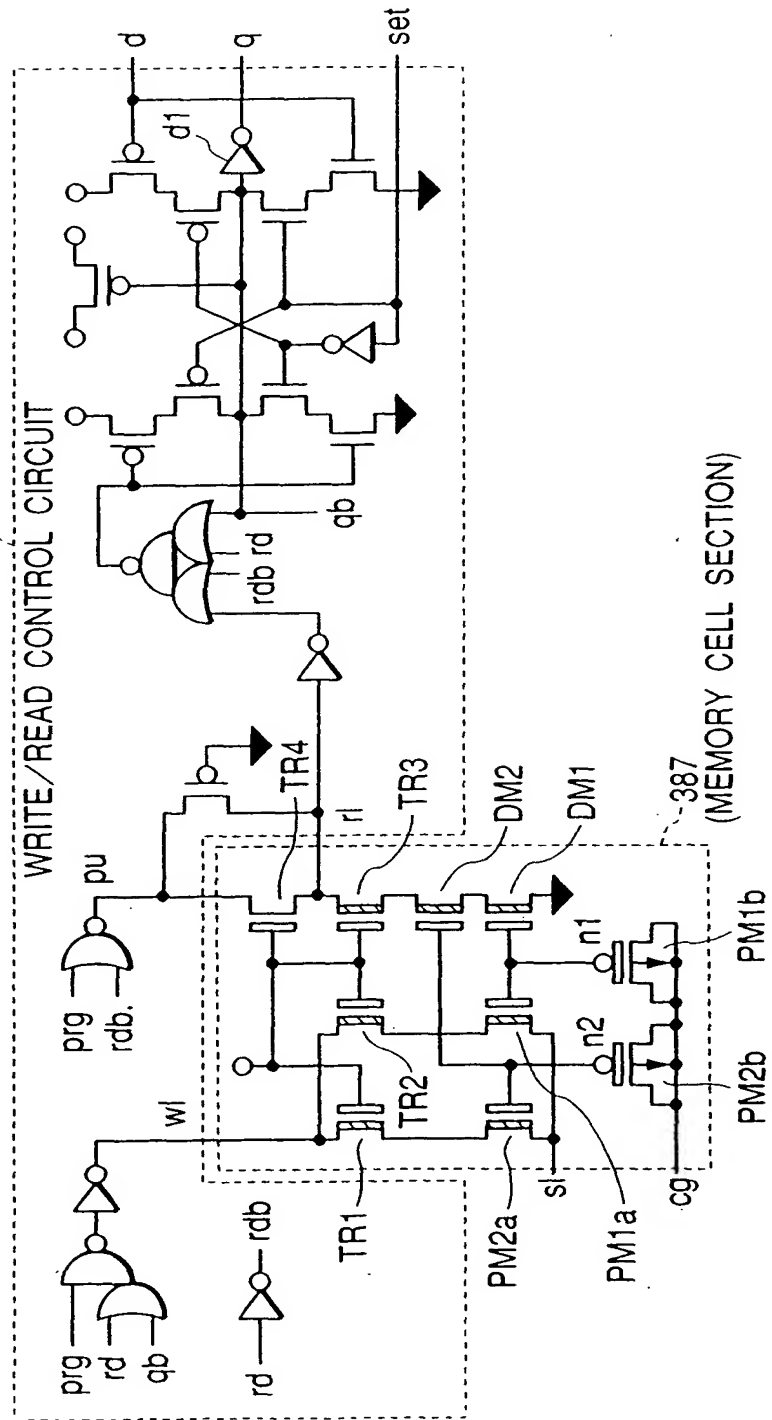
**FIG. 42**

FIG. 43

	rd	prg	set	d	cg	sl	pu	wl	n	rl	q
inh	x	1.5	1.5								
	1.5	x									
data set	"0"	0	0	0	0	0	0	0	x	0	0
	"1"			1.5							1.5
erase	"0"	2	2	0	5	0	0	2	0	0	0
	"1"							2	-5→0	0	0
prog	"0"	0	2	5	5	0	0	2	5	0	0
	"1"							0	5→0	0	2
read	"0"	1.5	0	1.5	0	1.5	1.5	0	1.5	0	0
	"1"							0	-3	1.5	1.5
(test)	"x"	1.5	0	ext	0	1.5	1.5	0	x	1/0	1/0
hold	"0"	0	0	0	0	0	0	0	x	0	0
	"1"										1.5

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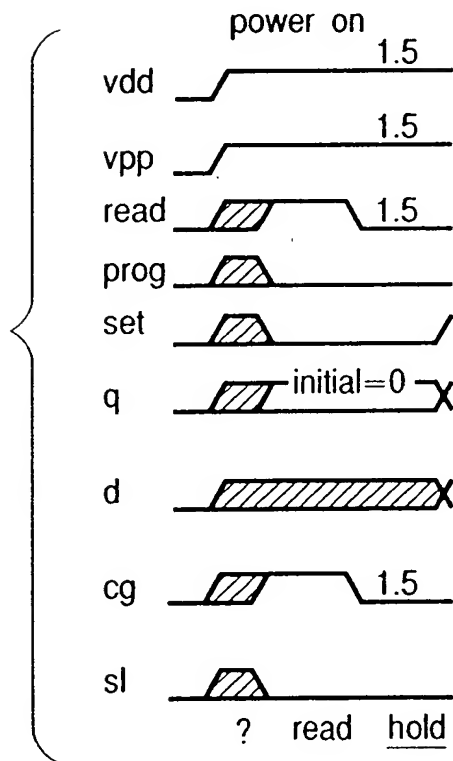
**FIG. 45**READ TIMING CHART  
IN ACTUAL USE

FIG. 46

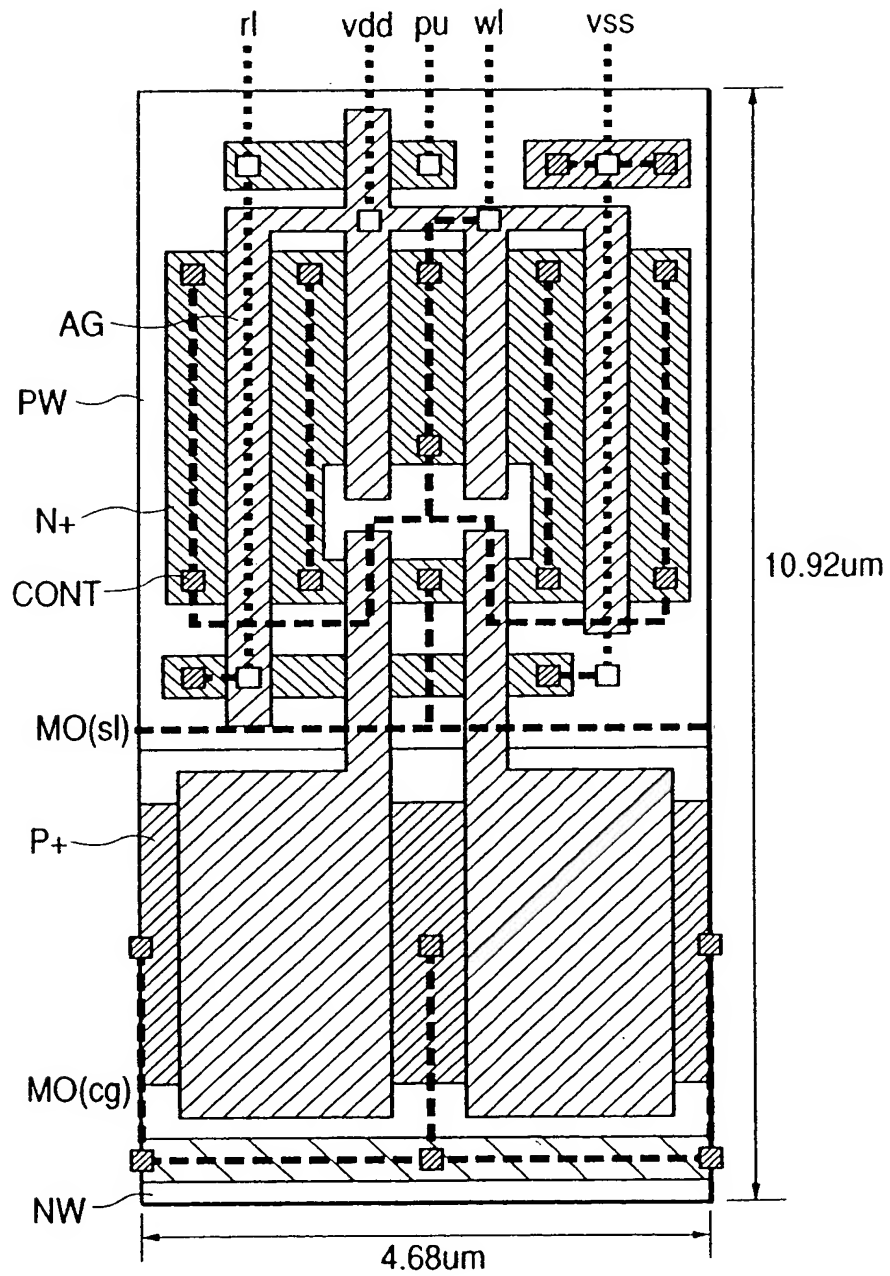




FIG. 47

FUSE CONTROL WAVEFORM

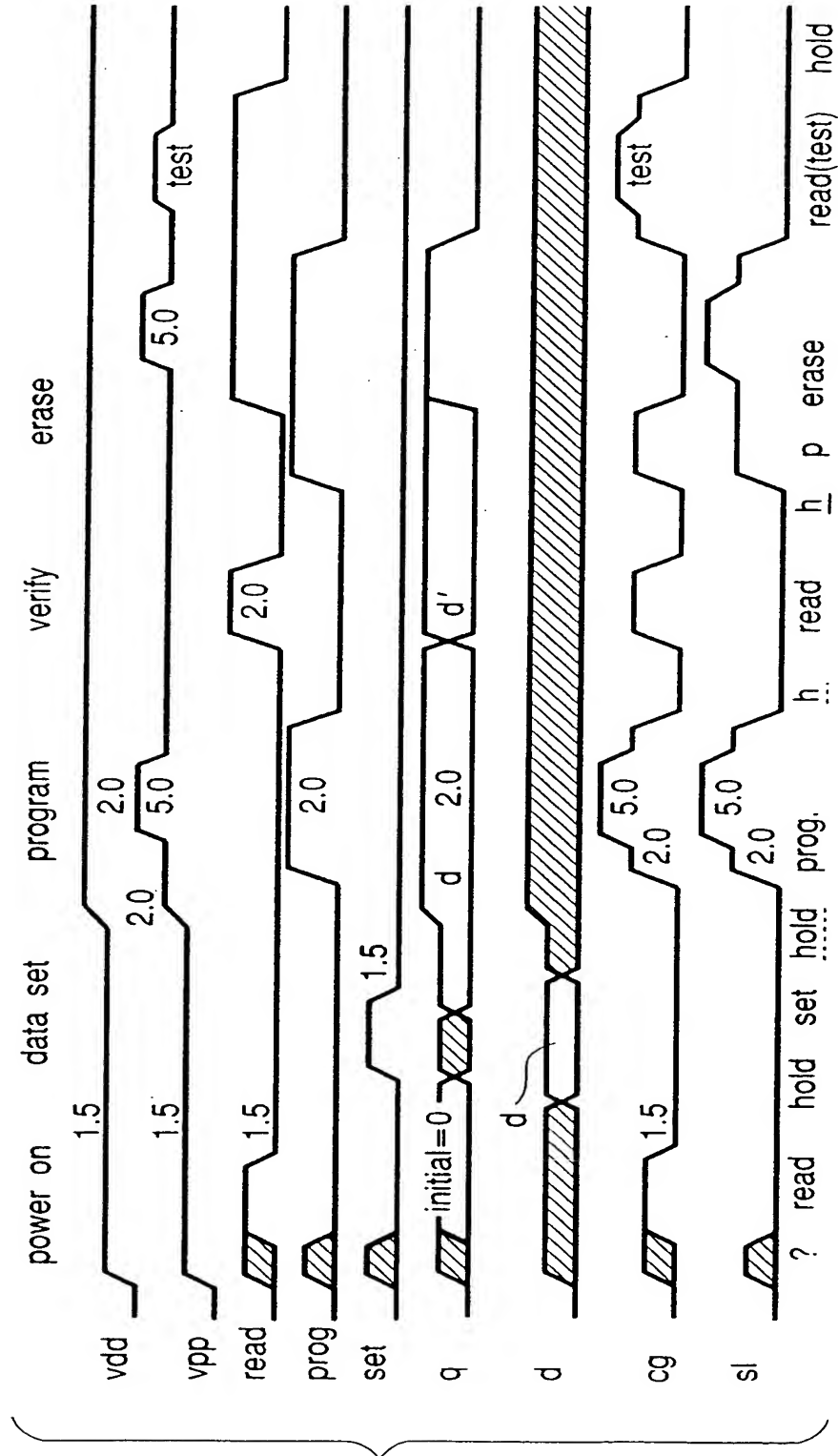
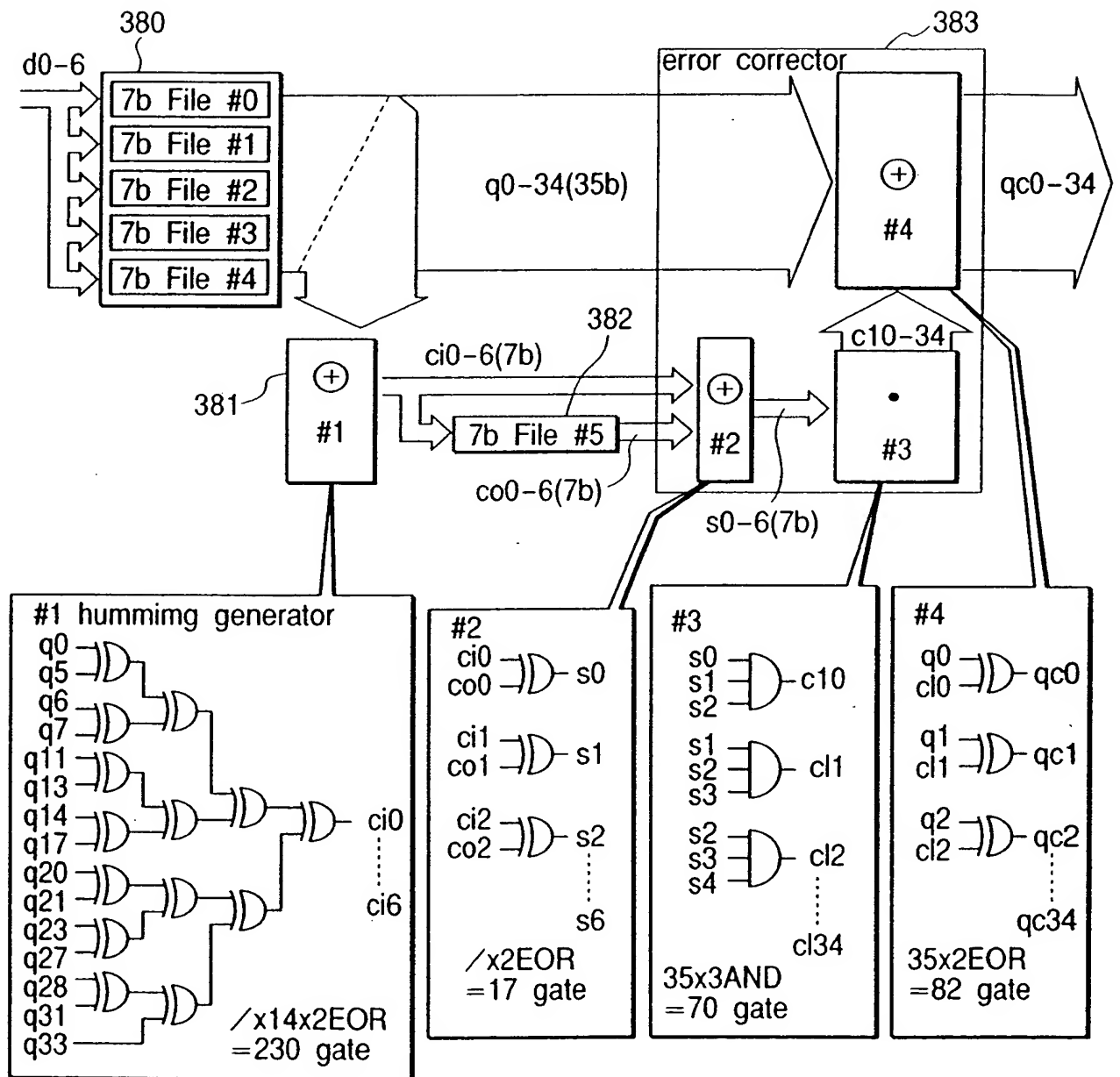
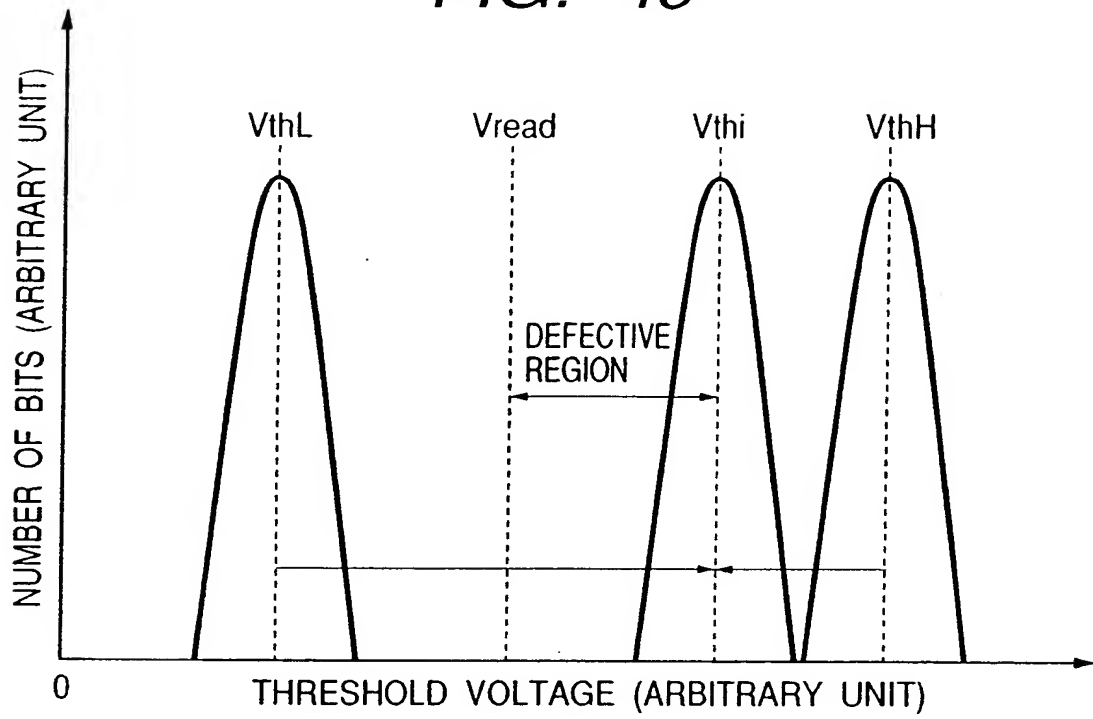
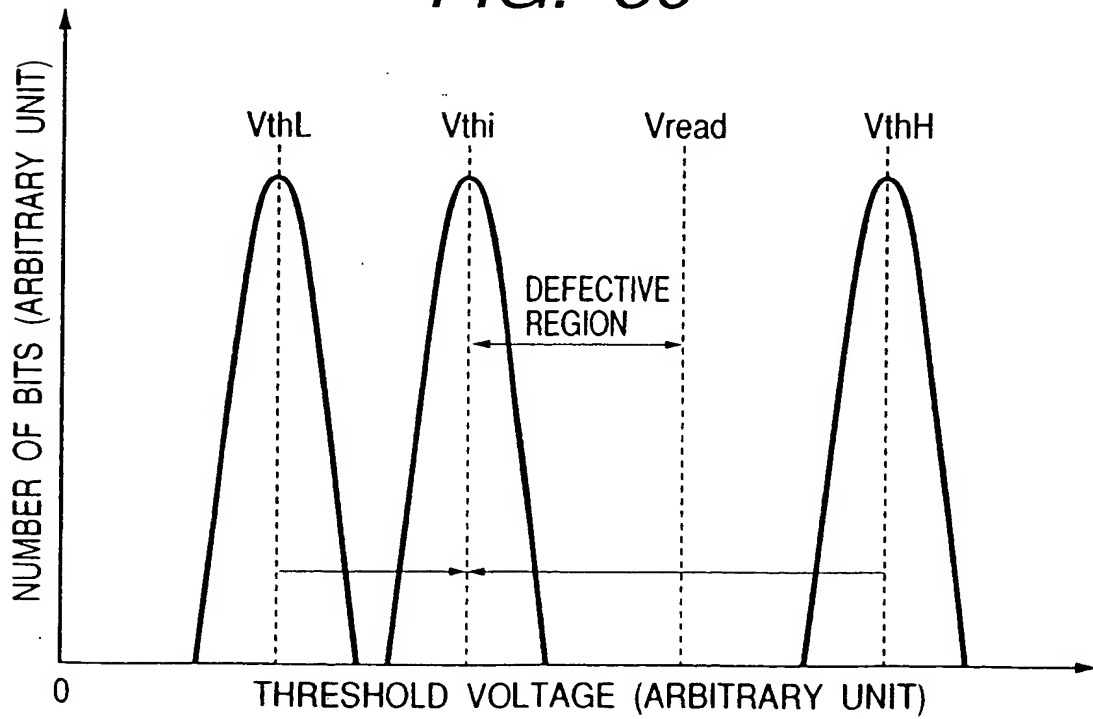


FIG. 48



*FIG. 49**FIG. 50*

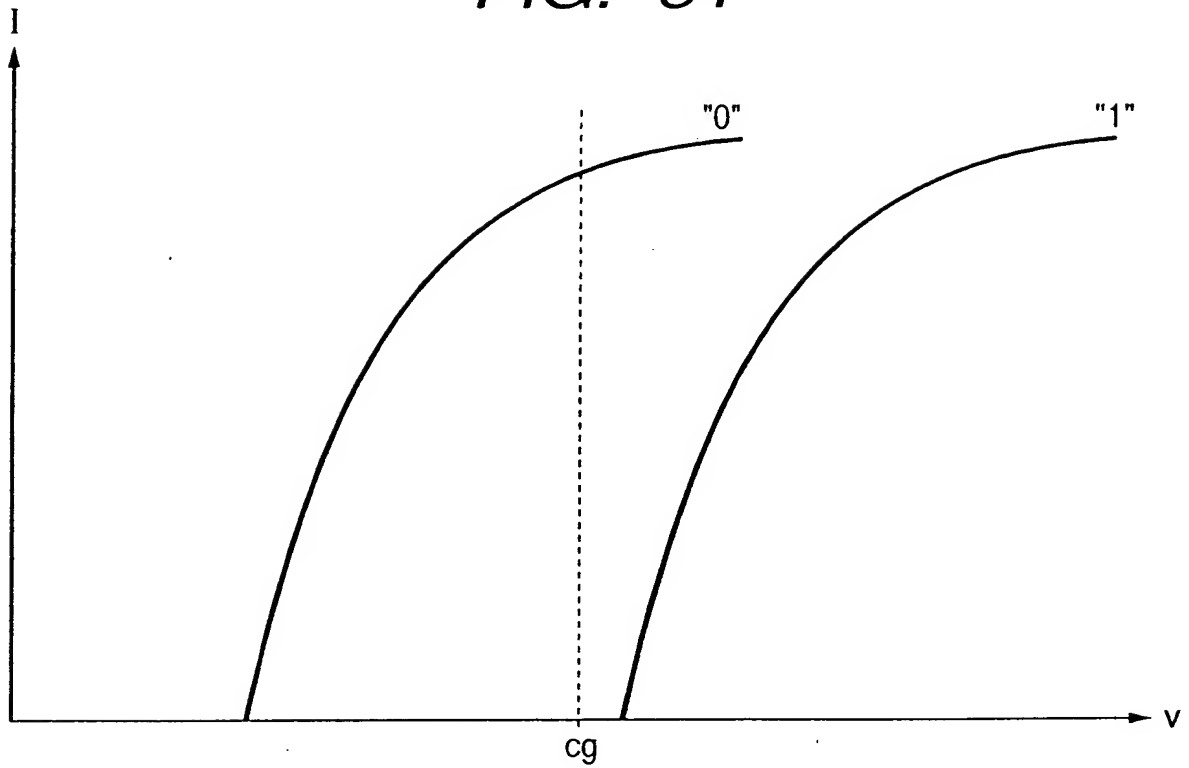
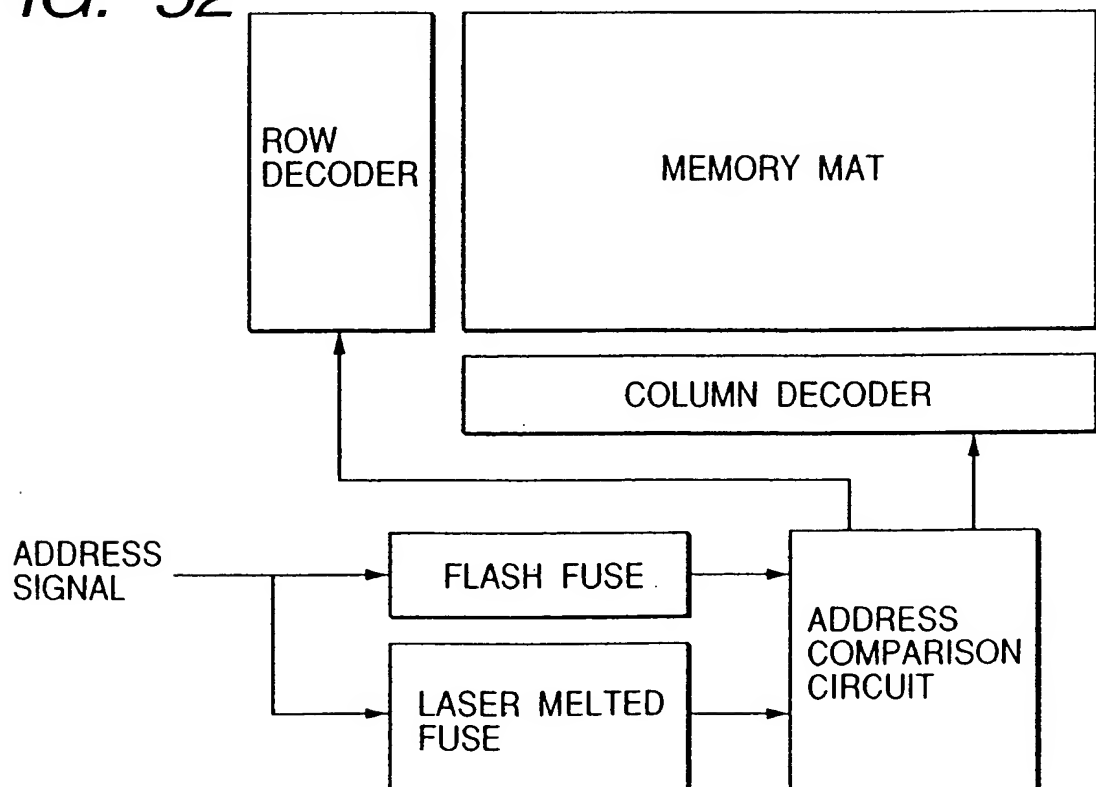
*FIG. 51**FIG. 52*

FIG. 53

CROSS-SECTIONAL VIEW OF DRAM CELL

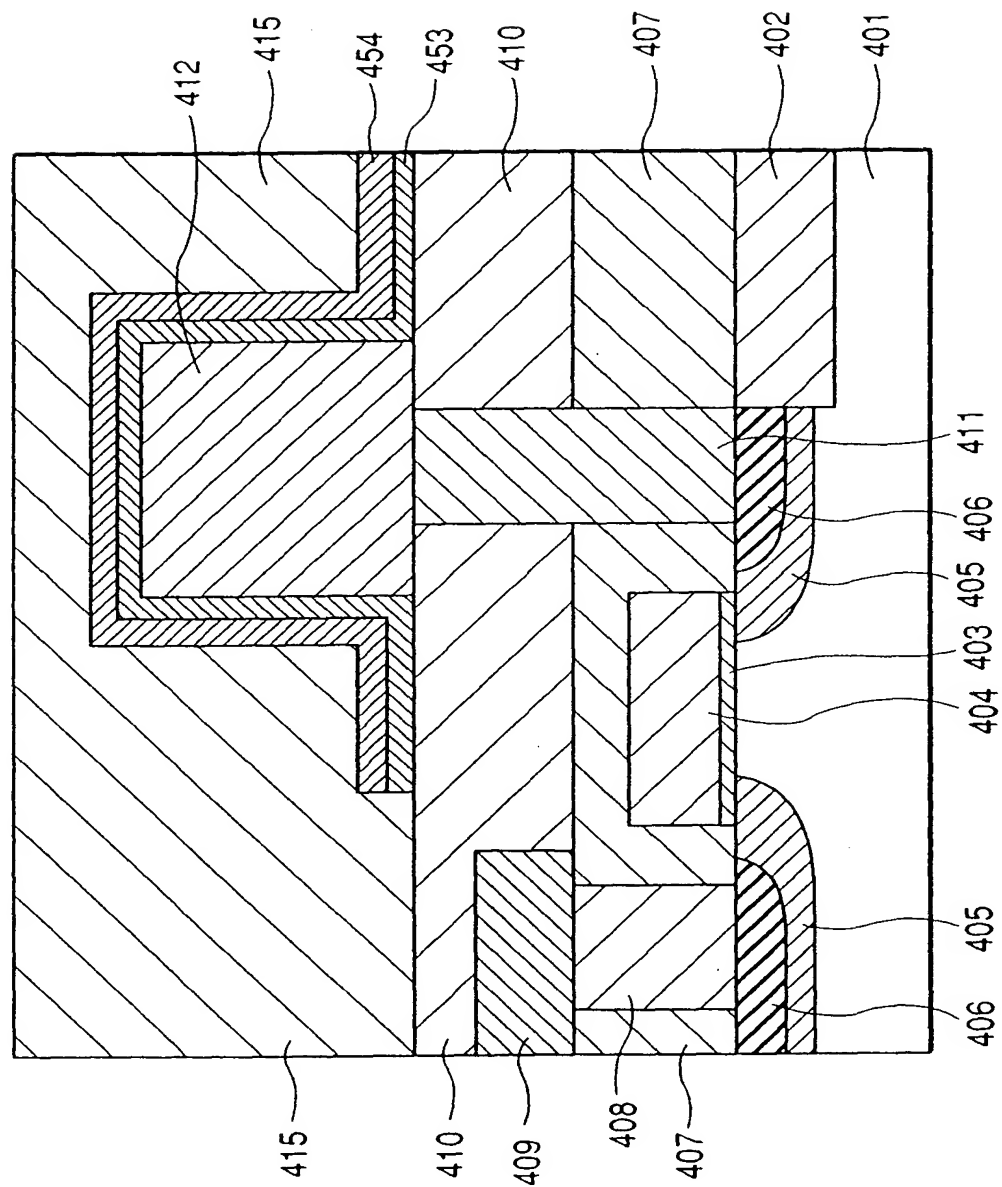


FIG. 54

